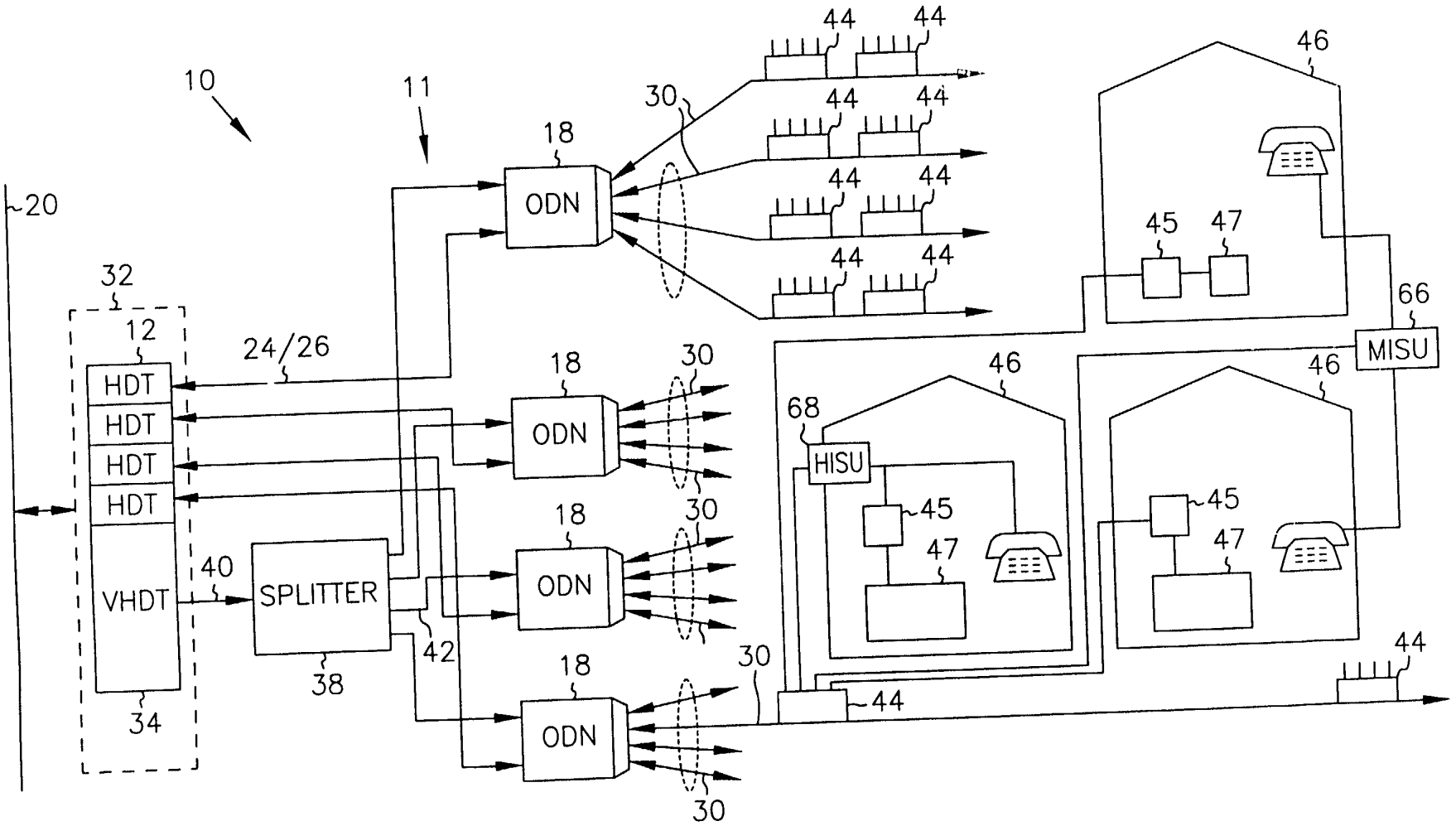

10
11
20
32
12
HDT
HDT
HDT
HDT
VHDT
24/26
34
40
SPLITTER
38
42
18
ODN
18
ODN
18
ODN
30
30
30
30
44
44
44
44
44
44
44
44
46
45
47
66
MISU
46
68
HISU
45
47
46
45
47
44
44

FIG. 1

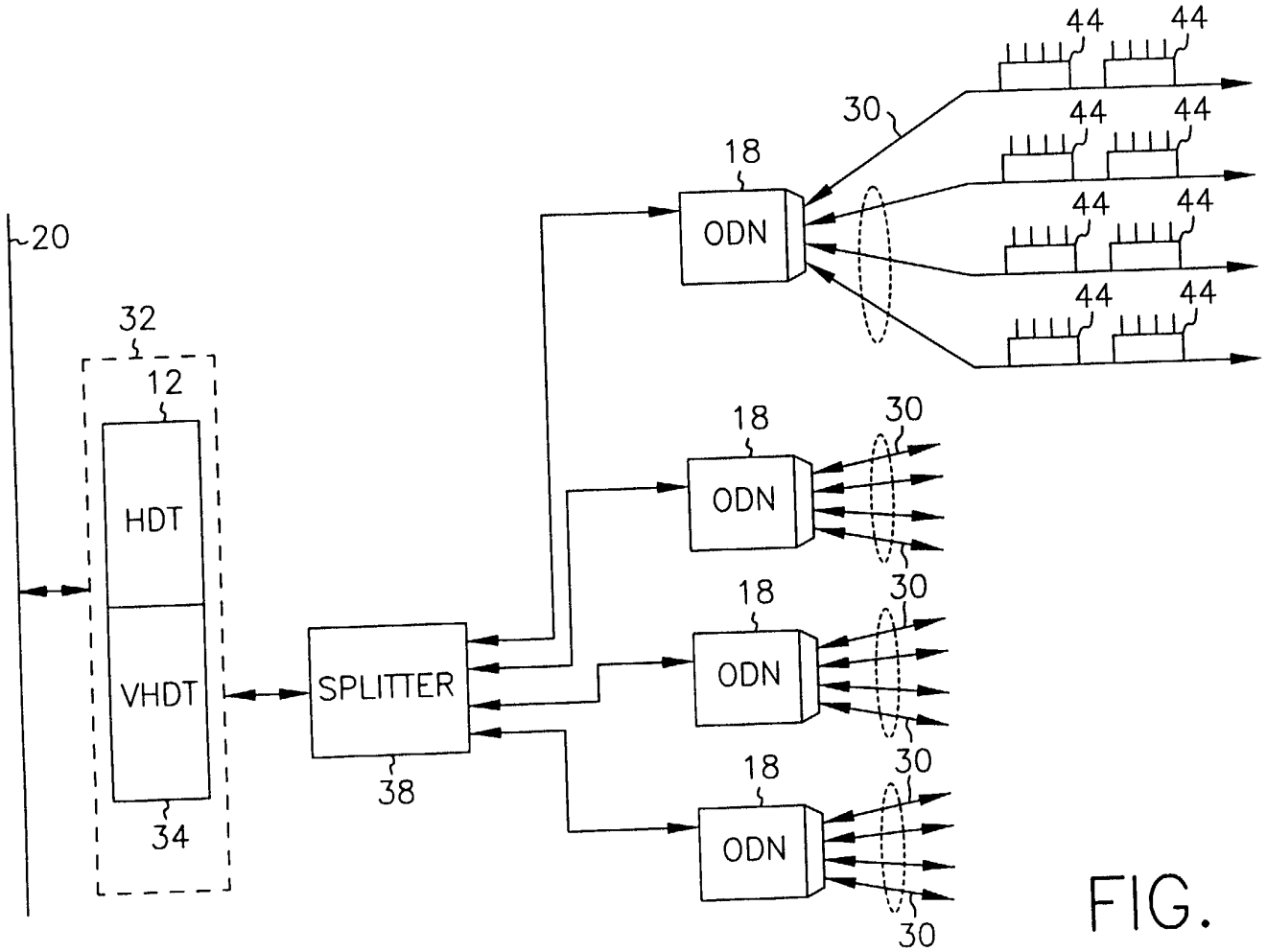


FIG. 2

0990537A "070901

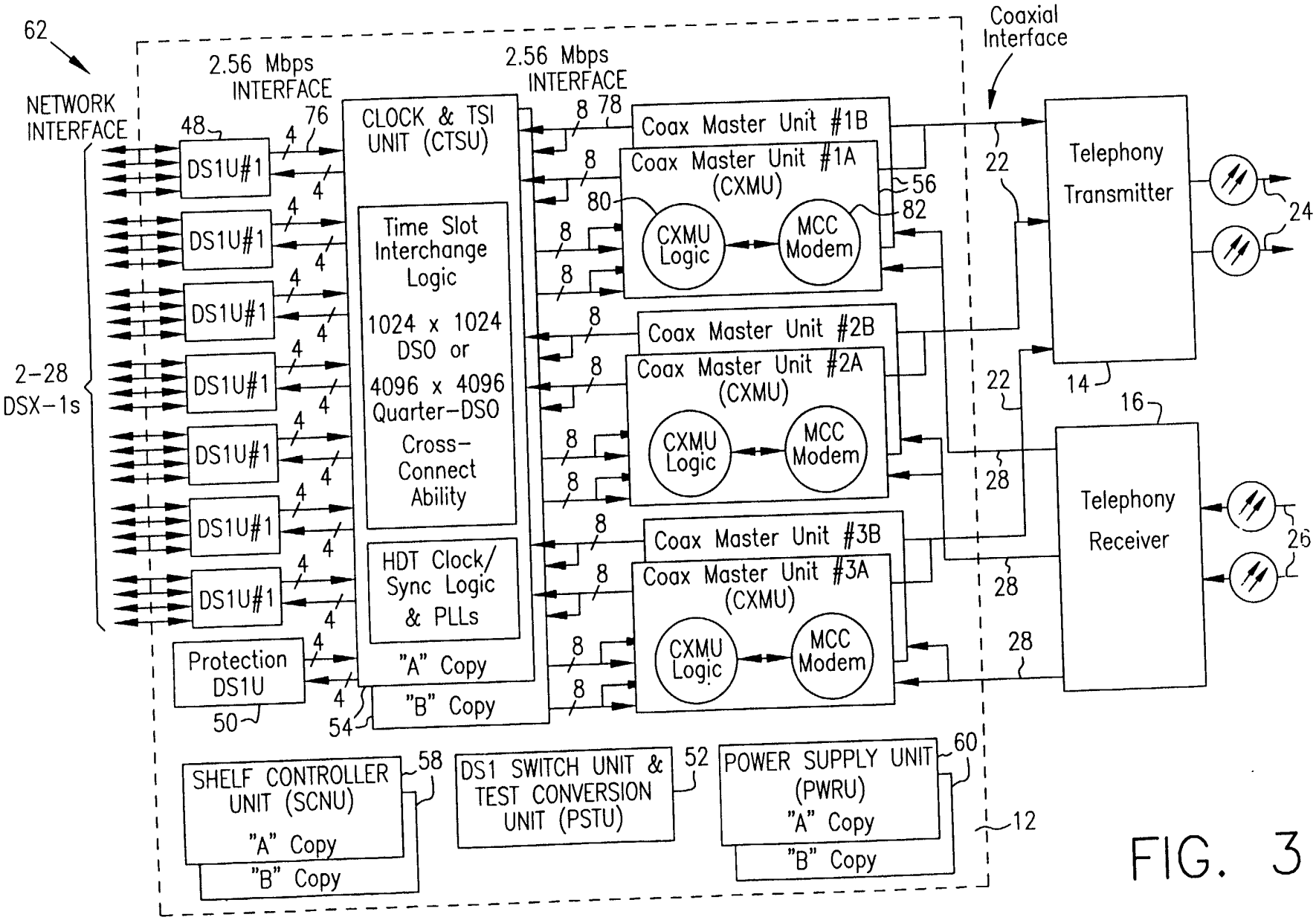
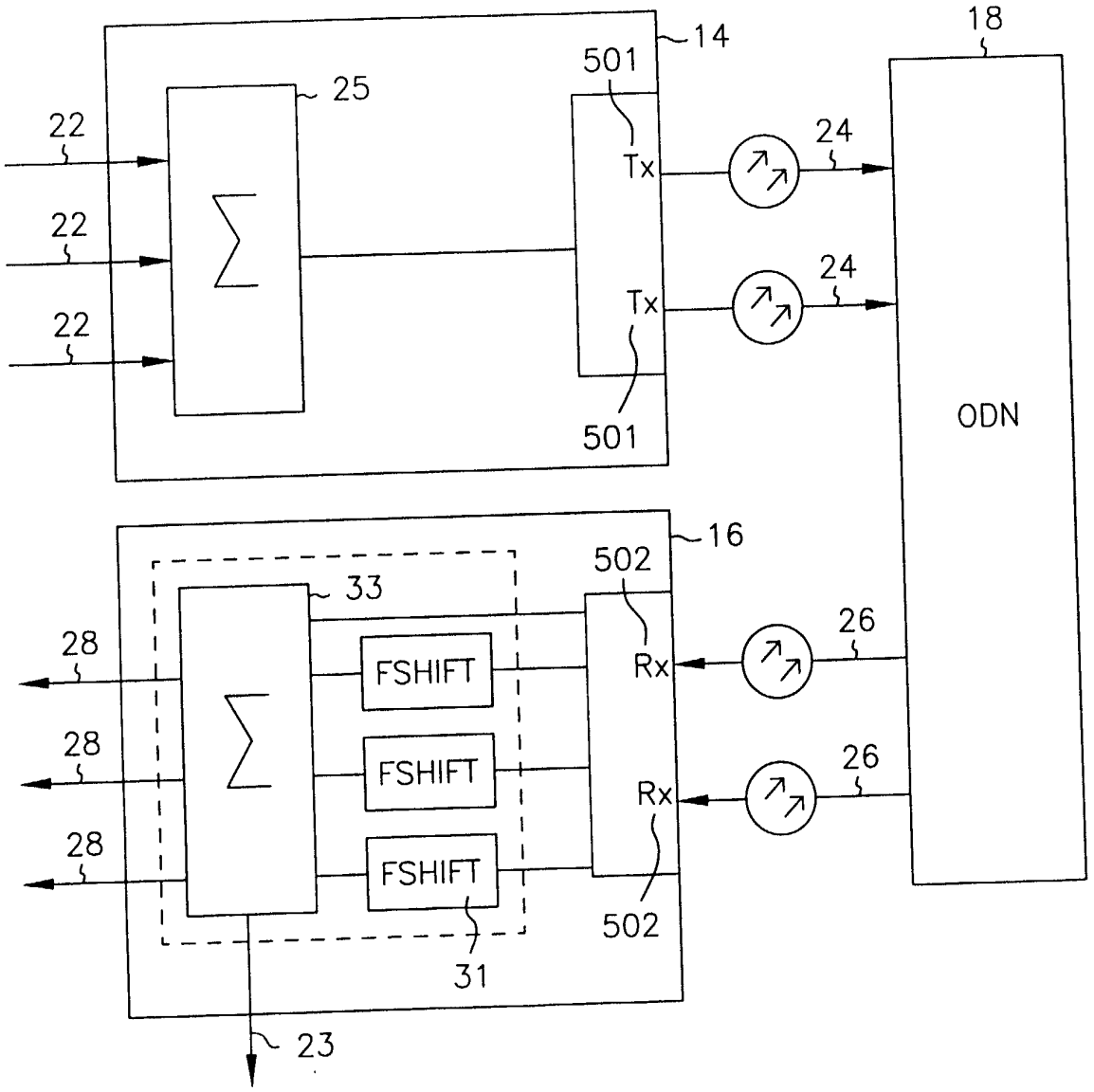


FIG. 3

TD60Z0"h2ETD660

FIG. 4



T06020"A2ET0660

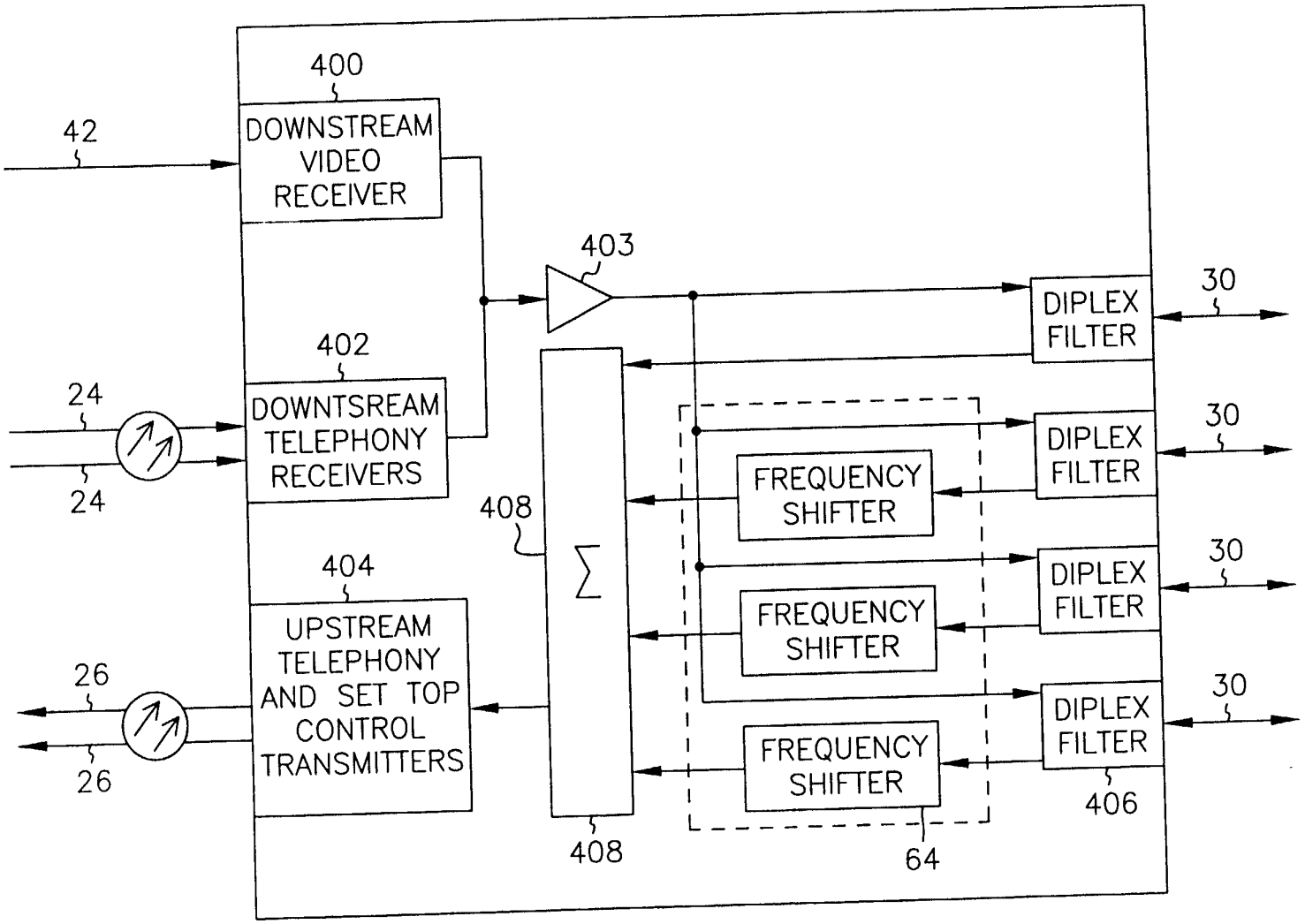


FIG. 5

FIG. 6

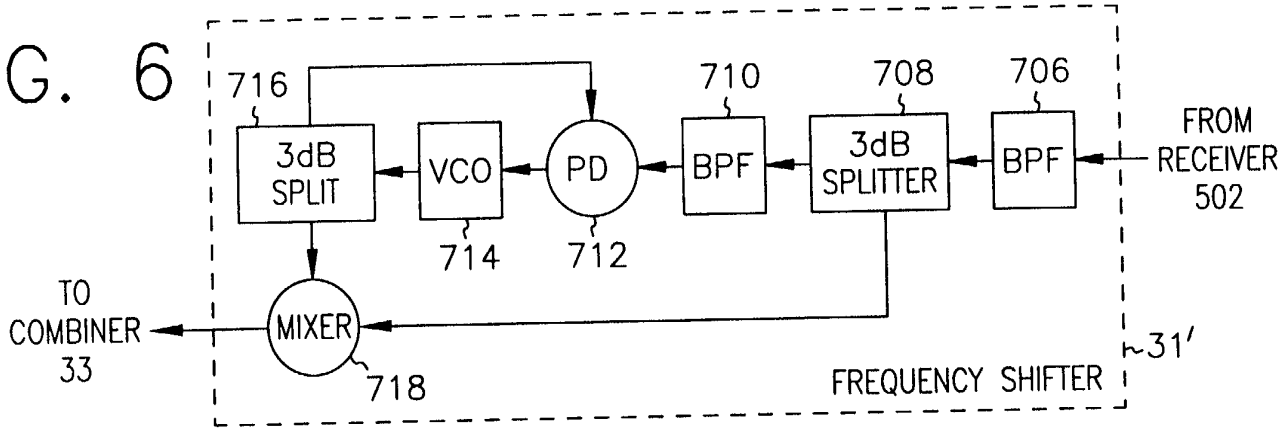
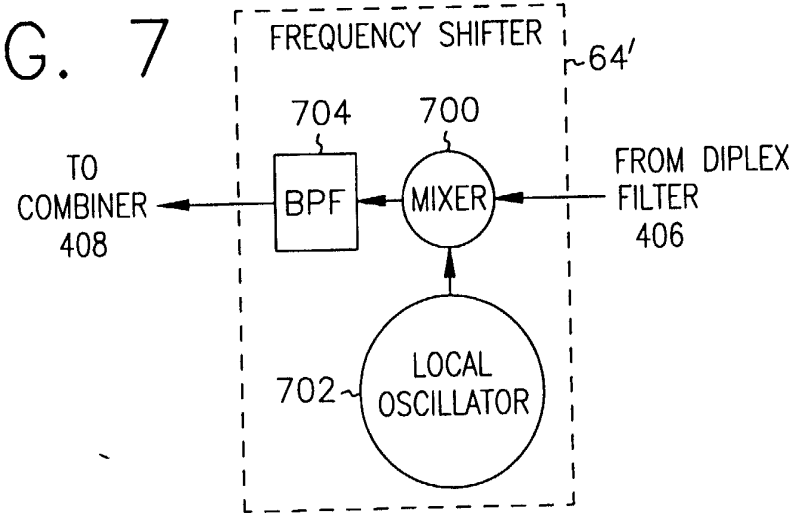

716
710
708
706
3dB SPLIT
VCO
PD
BPF
3dB SPLITTER
BPF
FROM RECEIVER 502
714
712
TO COMBINER 33
MIXER
718
31'
FREQUENCY SHIFTER

FIG. 7


FREQUENCY SHIFTER
64'
704
700
TO COMBINER 408
BPF
MIXER
FROM DIPLEX FILTER 406
LOCAL OSCILLATOR
702

TOSOZO "WZETOOSO

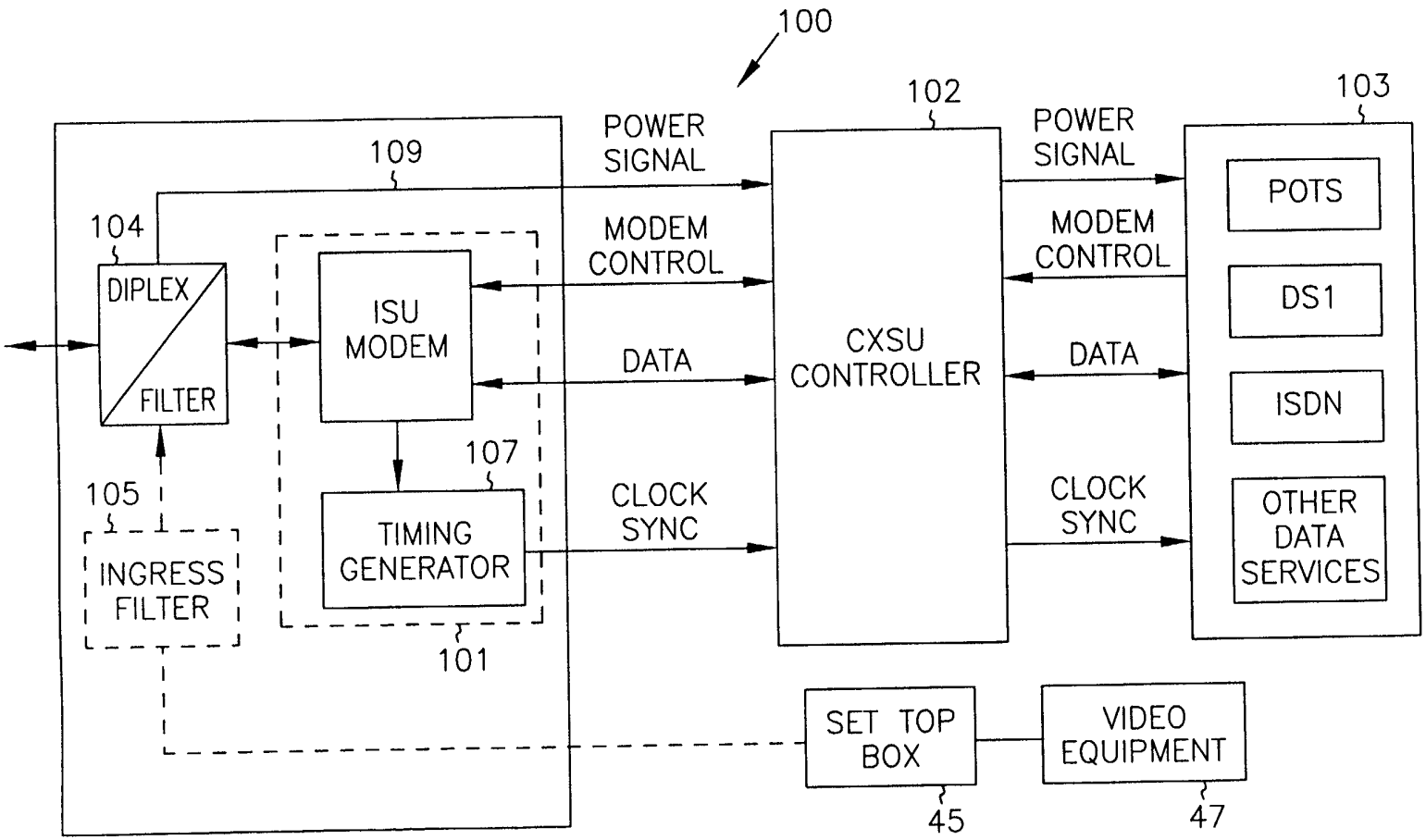


FIG. 8

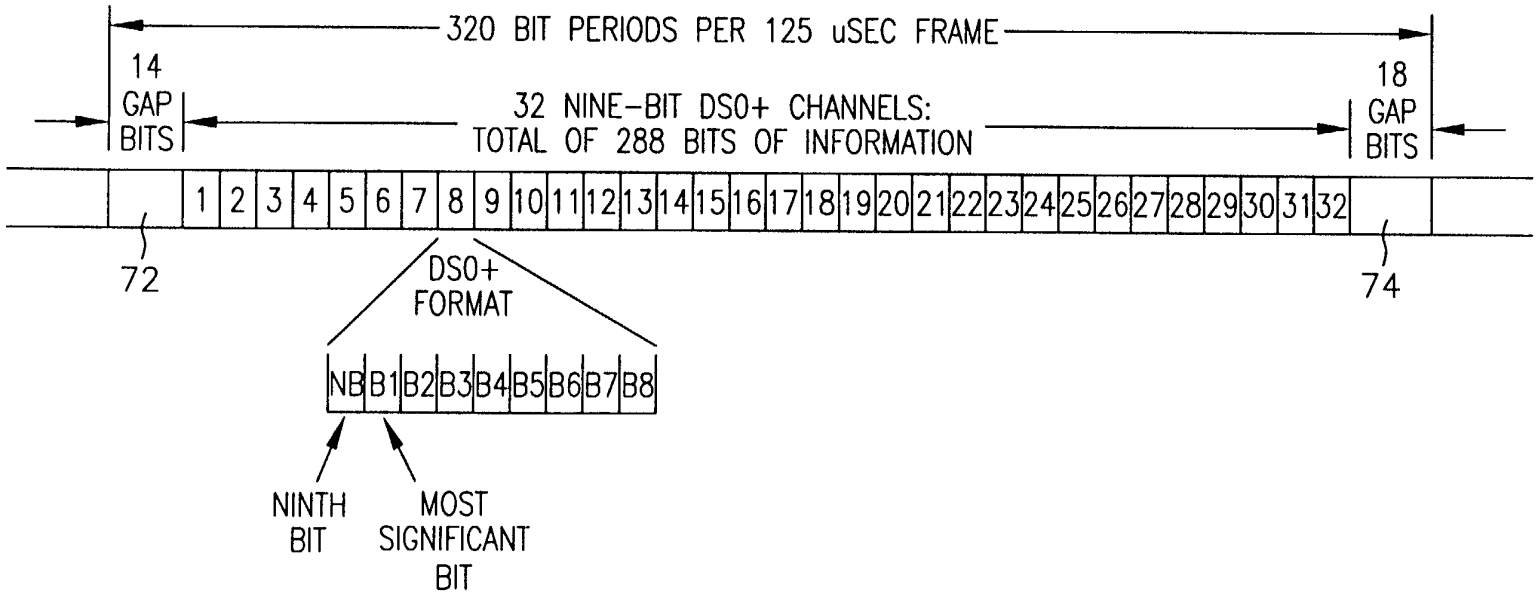

320 BIT PERIODS PER 125 uSEC FRAME
14 GAP BITS
32 NINE-BIT DS0+ CHANNELS: TOTAL OF 288 BITS OF INFORMATION
18 GAP BITS
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
72
74
DS0+ FORMAT
NB B1 B2 B3 B4 B5 B6 B7 B8
NINTH BIT
MOST SIGNIFICANT BIT

FIG. 9

T0602D" h2ET0660

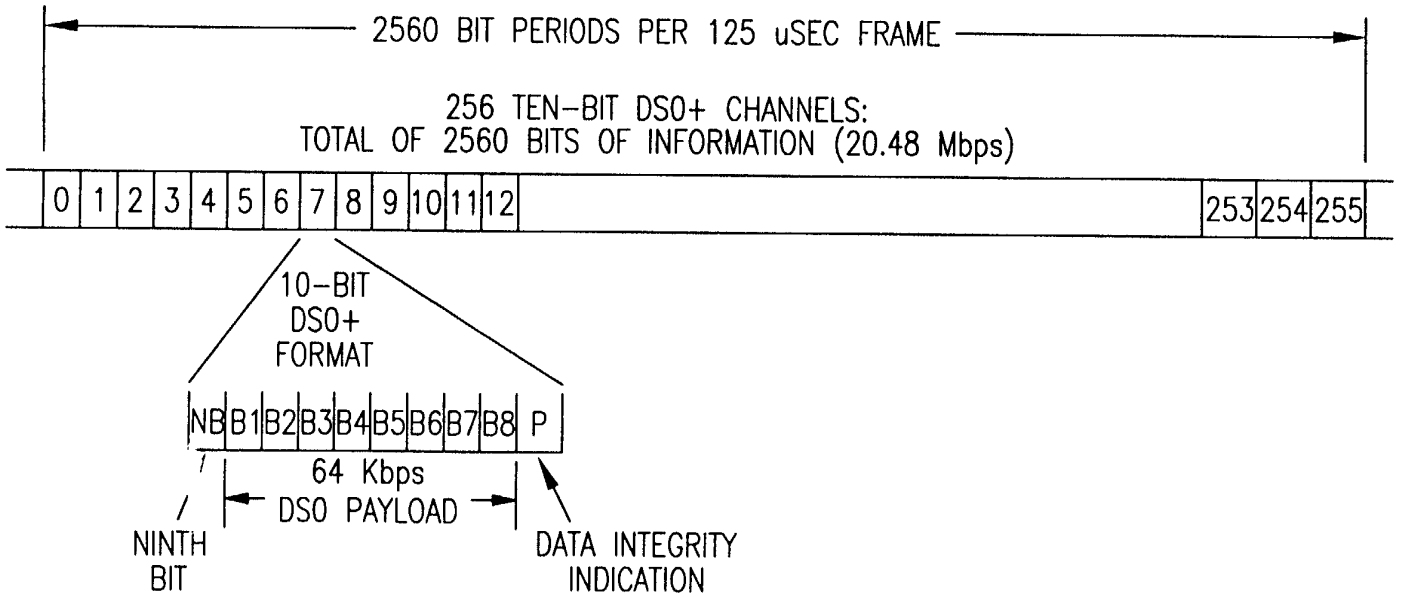


FIG. 10

TD6020 "WZ97060

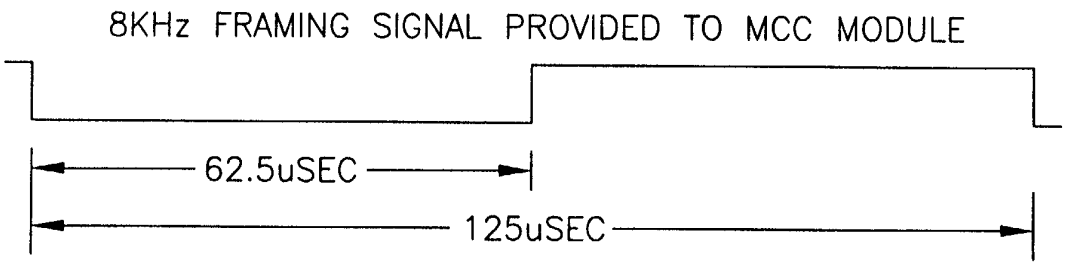


FIG. 11

TD60270 "4/2/96

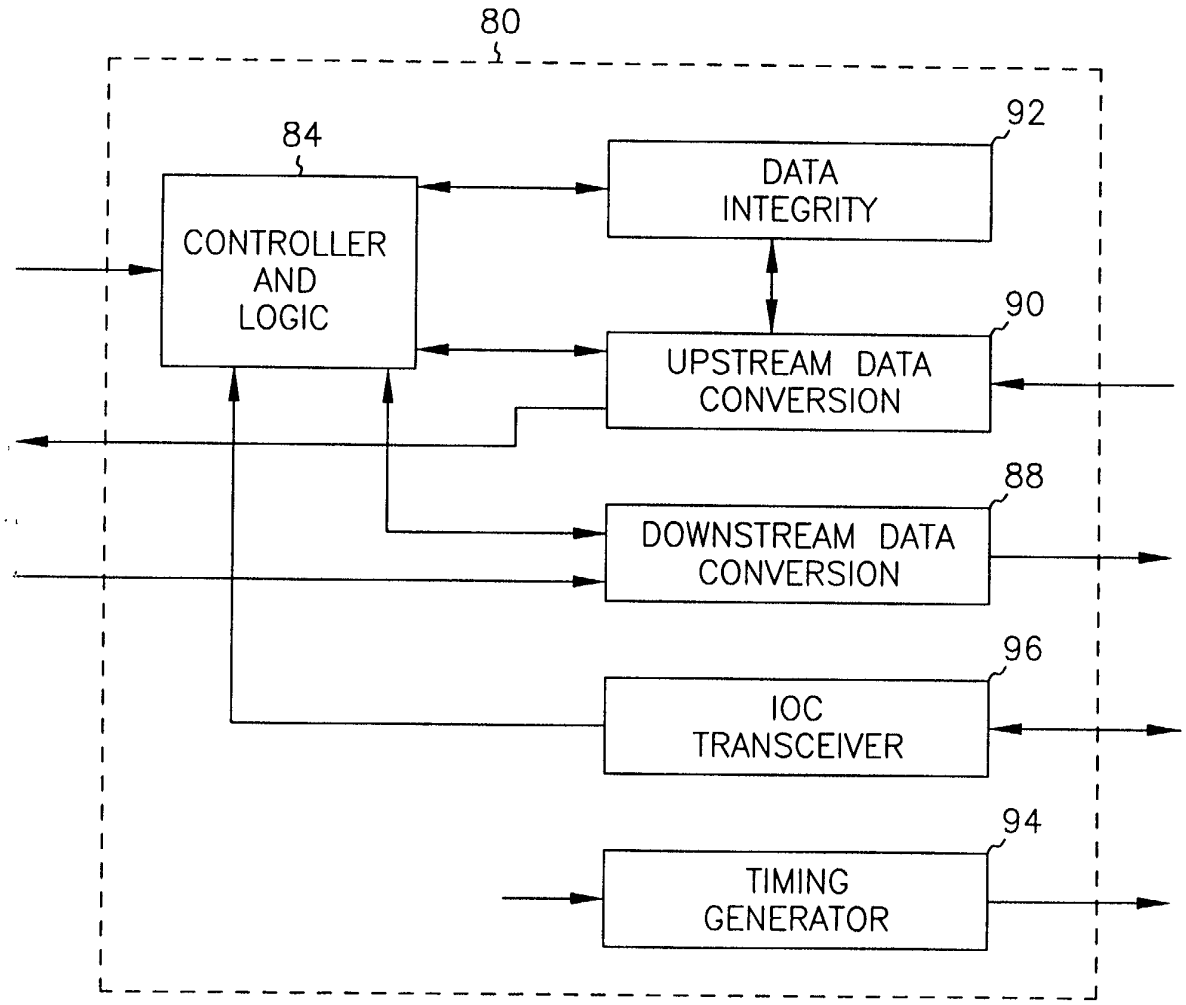


FIG. 12

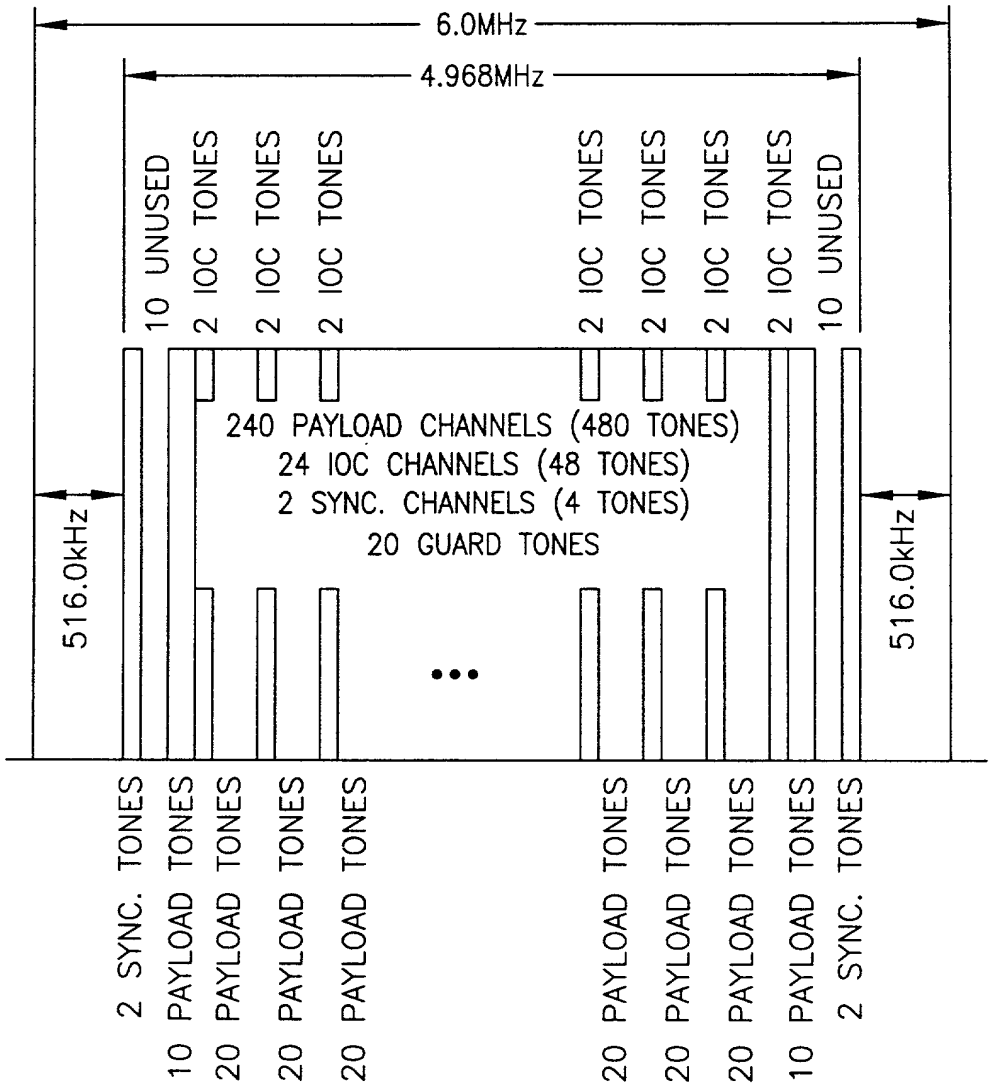

6.0MHz
4.968MHz
10 UNUSED
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
10 UNUSED
240 PAYLOAD CHANNELS (480 TONES)
24 IOC CHANNELS (48 TONES)
2 SYNC. CHANNELS (4 TONES)
20 GUARD TONES
516.0kHz
516.0kHz
2 SYNC. TONES
10 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
10 PAYLOAD TONES
2 SYNC. TONES

FIG. 13

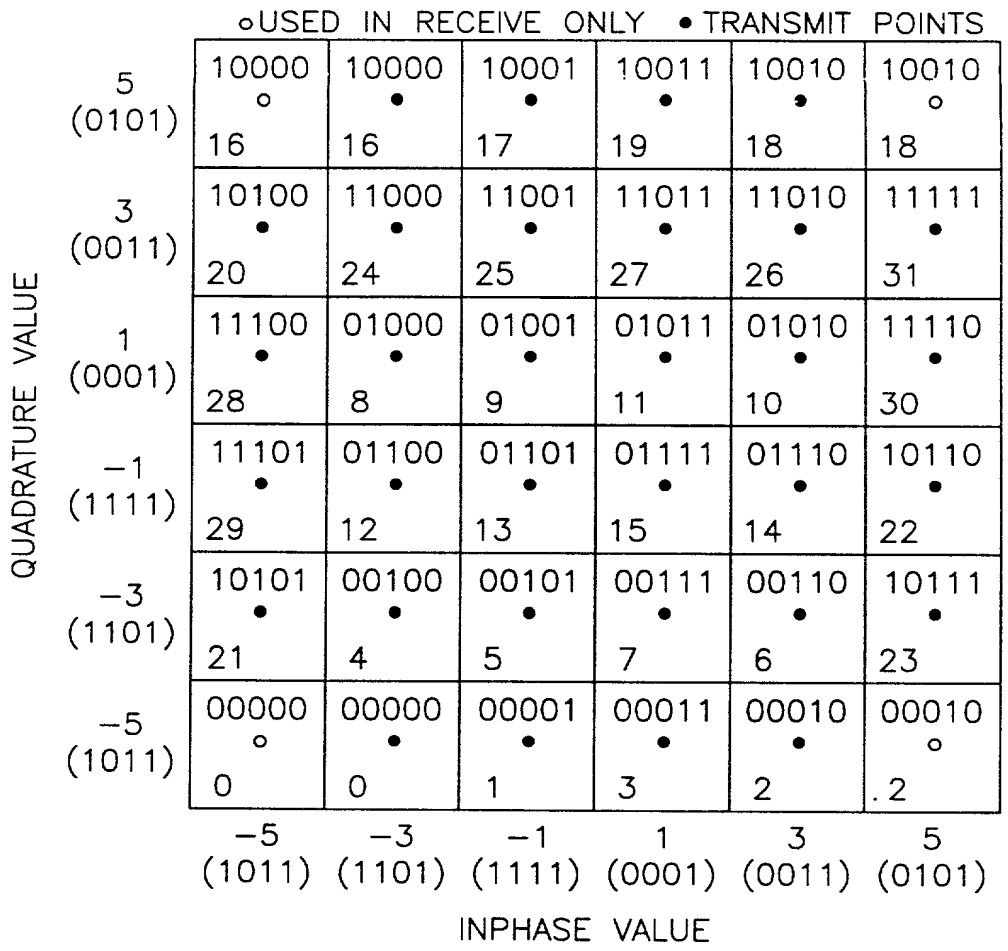

o USED IN RECEIVE ONLY • TRANSMIT POINTS
QUADRATURE VALUE
5 (0101)
3 (0011)
1 (0001)
−1 (1111)
−3 (1101)
−5 (1011)
10000 16 | 10000 16 | 10001 17 | 10011 19 | 10010 18 | 10010 18
10100 20 | 11000 24 | 11001 25 | 11011 27 | 11010 26 | 11111 31
11100 28 | 01000 8 | 01001 9 | 01011 11 | 01010 10 | 11110 30
11101 29 | 01100 12 | 01101 13 | 01111 15 | 01110 14 | 10110 22
10101 21 | 00100 4 | 00101 5 | 00111 7 | 00110 6 | 10111 23
00000 0 | 00000 0 | 00001 1 | 00011 3 | 00010 2 | 00010 .2
−5 (1011) −3 (1101) −1 (1111) 1 (0001) 3 (0011) 5 (0101)
INPHASE VALUE

FIG. 14

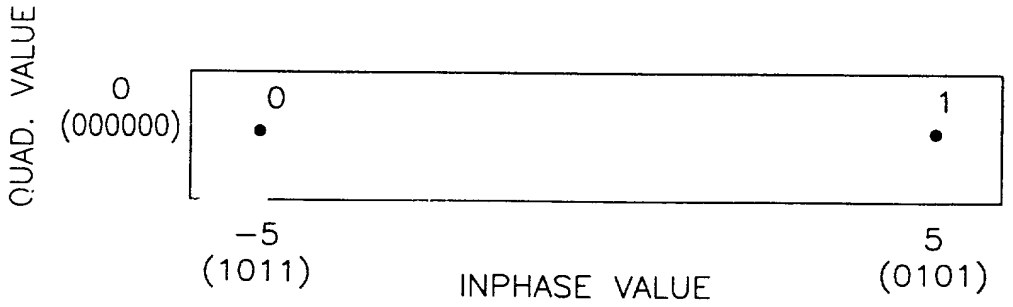

QUAD. VALUE
0 (000000)
0
1
−5 (1011)
5 (0101)
INPHASE VALUE

FIG. 15

T060Z0"h2ET066Q

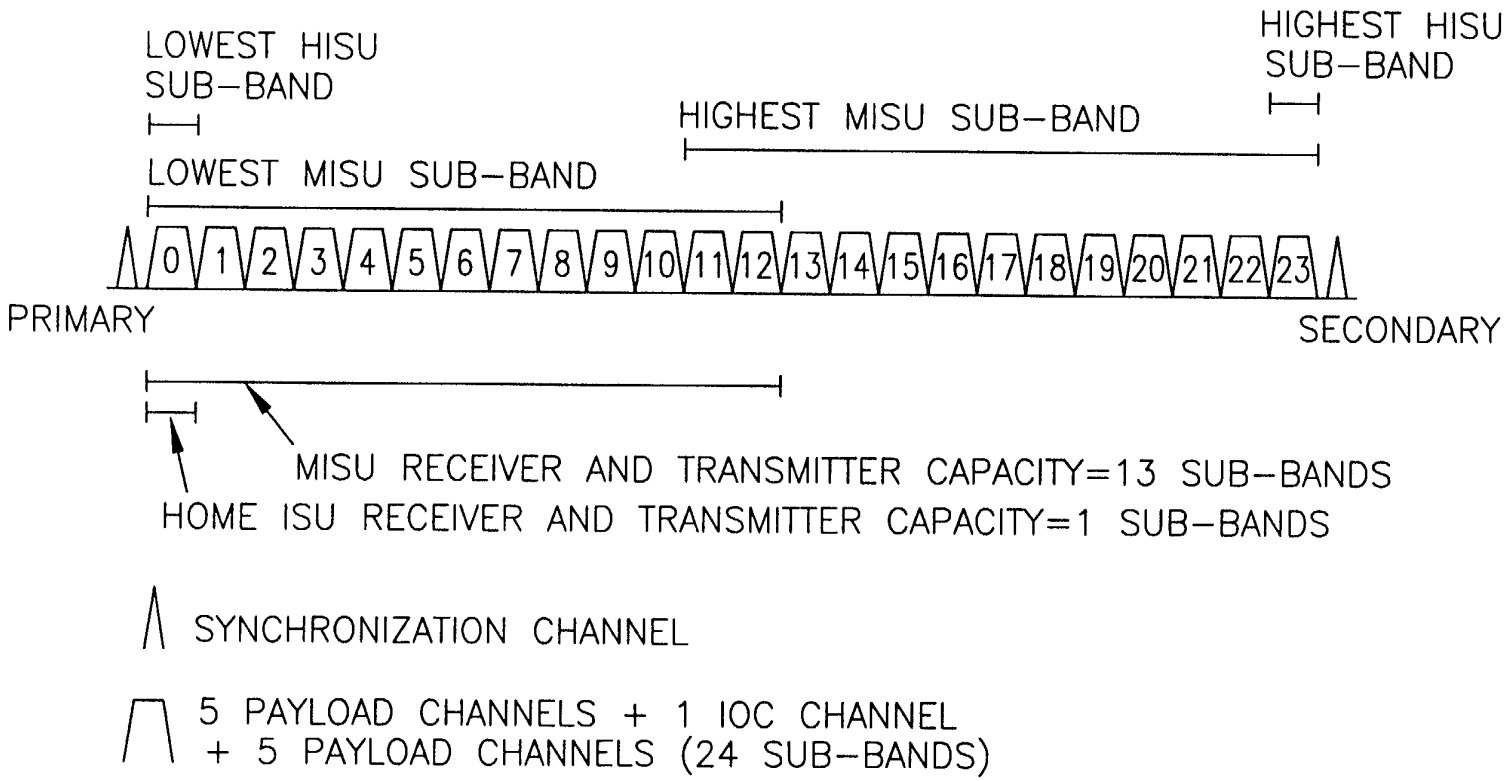


FIG. 16

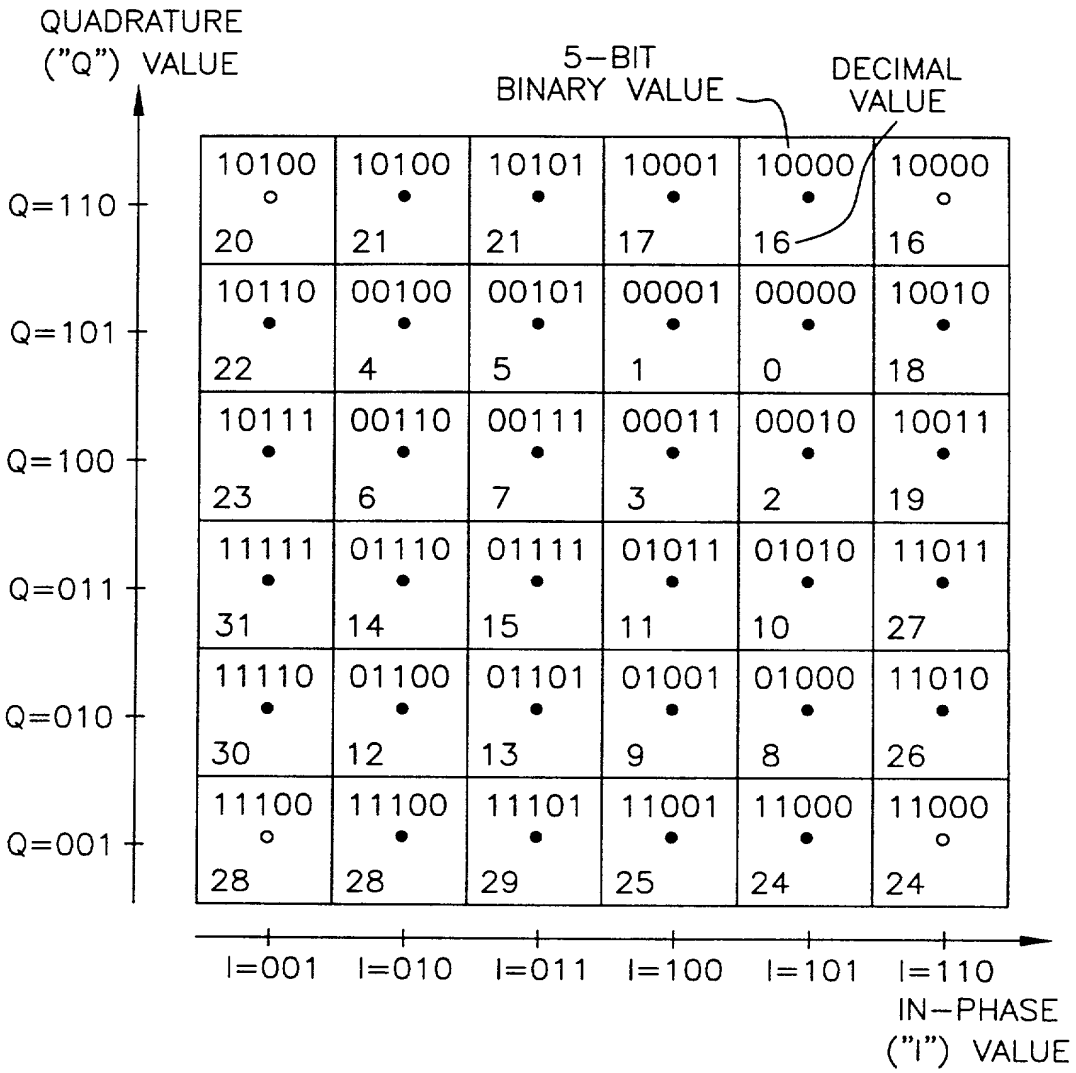

QUADRATURE
("Q") VALUE
5-BIT
BINARY VALUE
DECIMAL
VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE
("I") VALUE

FIG. 17

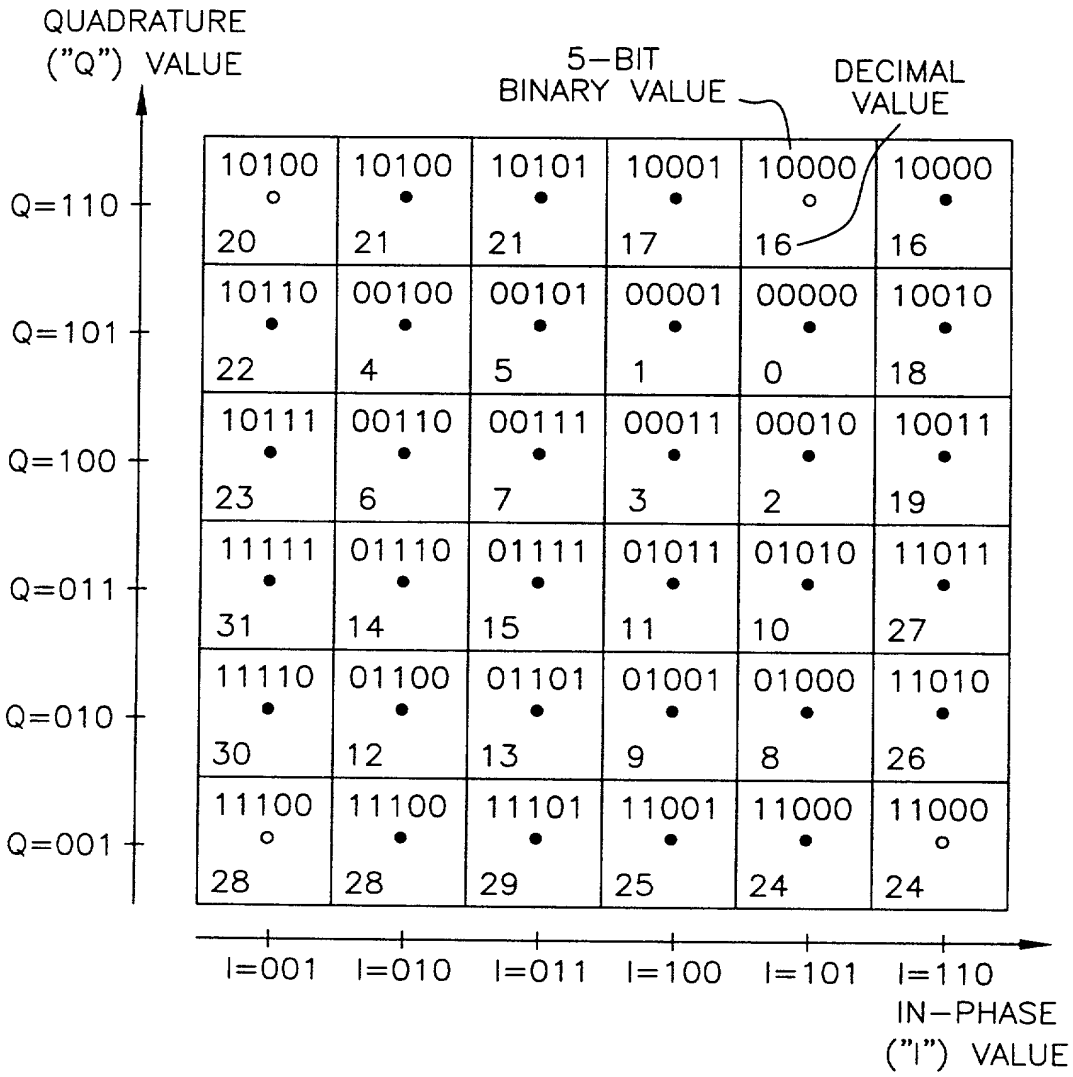

QUADRATURE ("Q") VALUE
5-BIT BINARY VALUE
DECIMAL VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE ("I") VALUE

FIG. 18

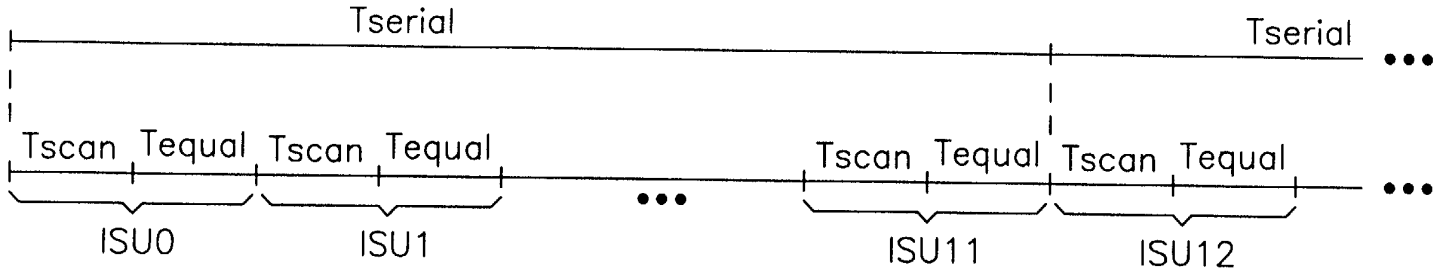

Tserial
Tserial
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
ISU0
ISU1
ISU11
ISU12

FIG. 19

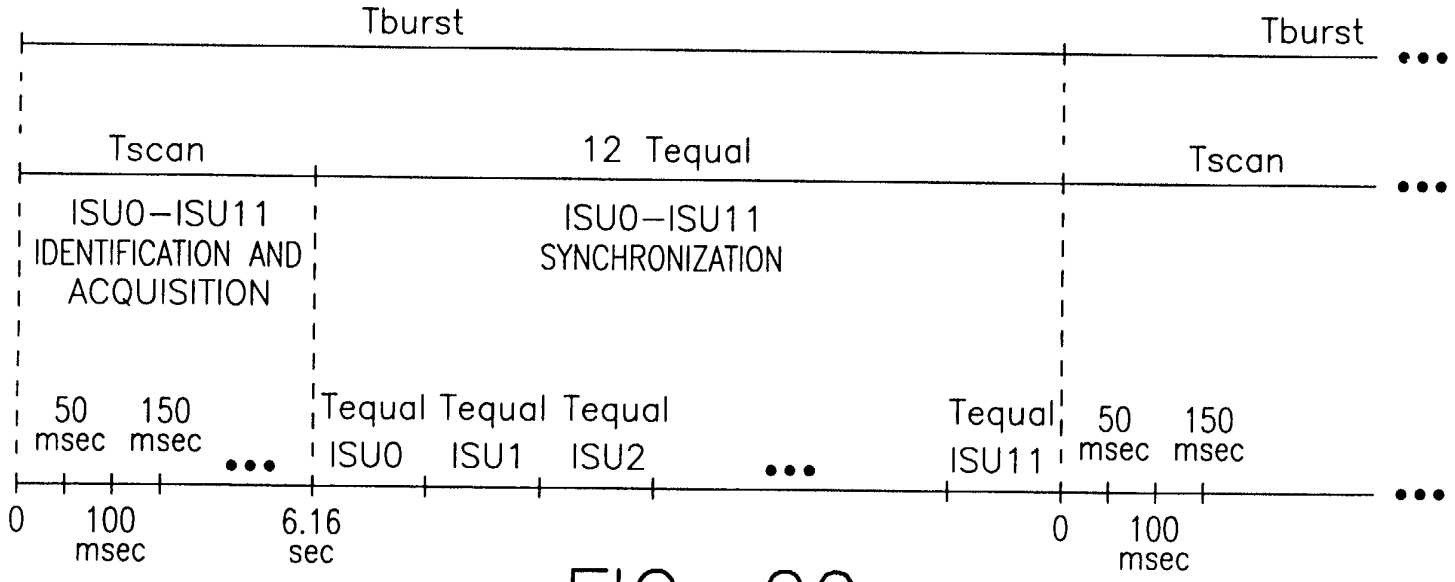

Tburst
Tburst
Tscan
12 Tequal
Tscan
ISU0–ISU11
IDENTIFICATION AND
ACQUISITION
ISU0–ISU11
SYNCHRONIZATION
50
msec
150
msec
Tequal
ISU0
Tequal
ISU1
Tequal
ISU2
Tequal
ISU11
50
msec
150
msec
0
100
msec
6.16
sec
0
100
msec

FIG. 20

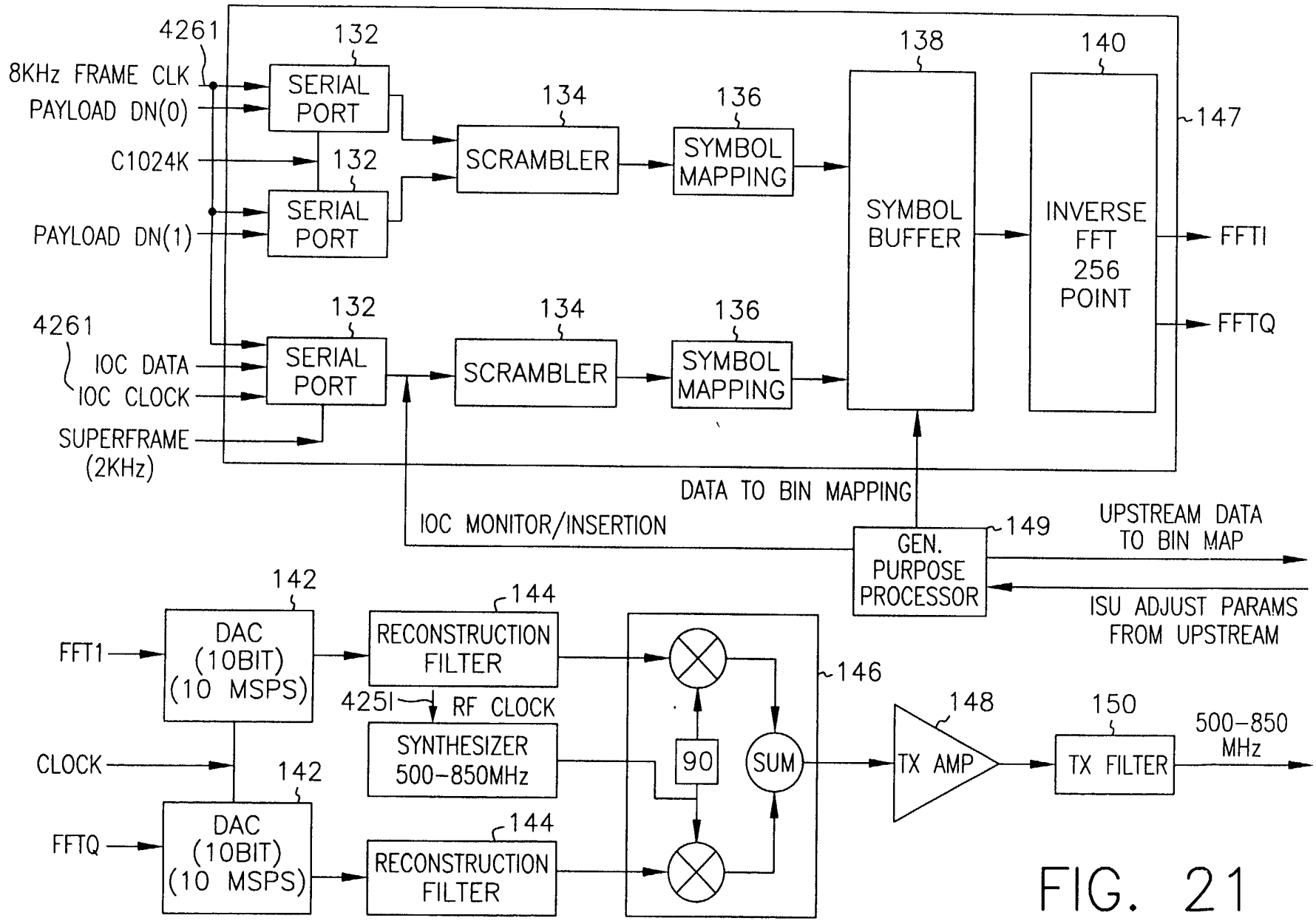

4261
8KHz FRAME CLK
PAYLOAD DN(0)
C1024K
PAYLOAD DN(1)
4261
IOC DATA
IOC CLOCK
SUPERFRAME (2KHz)
132
SERIAL PORT
132
SERIAL PORT
132
SERIAL PORT
134
SCRAMBLER
134
SCRAMBLER
136
SYMBOL MAPPING
136
SYMBOL MAPPING
138
SYMBOL BUFFER
140
INVERSE FFT 256 POINT
147
FFTI
FFTQ
DATA TO BIN MAPPING
IOC MONITOR/INSERTION
149
GEN. PURPOSE PROCESSOR
UPSTREAM DATA TO BIN MAP
ISU ADJUST PARAMS FROM UPSTREAM
142
DAC (10BIT) (10 MSPS)
144
RECONSTRUCTION FILTER
FFT1
4251
RF CLOCK
SYNTHESIZER 500-850MHz
CLOCK
142
DAC (10BIT) (10 MSPS)
144
RECONSTRUCTION FILTER
FFTQ
146
90
SUM
148
TX AMP
150
TX FILTER
500-850 MHz

FIG. 21

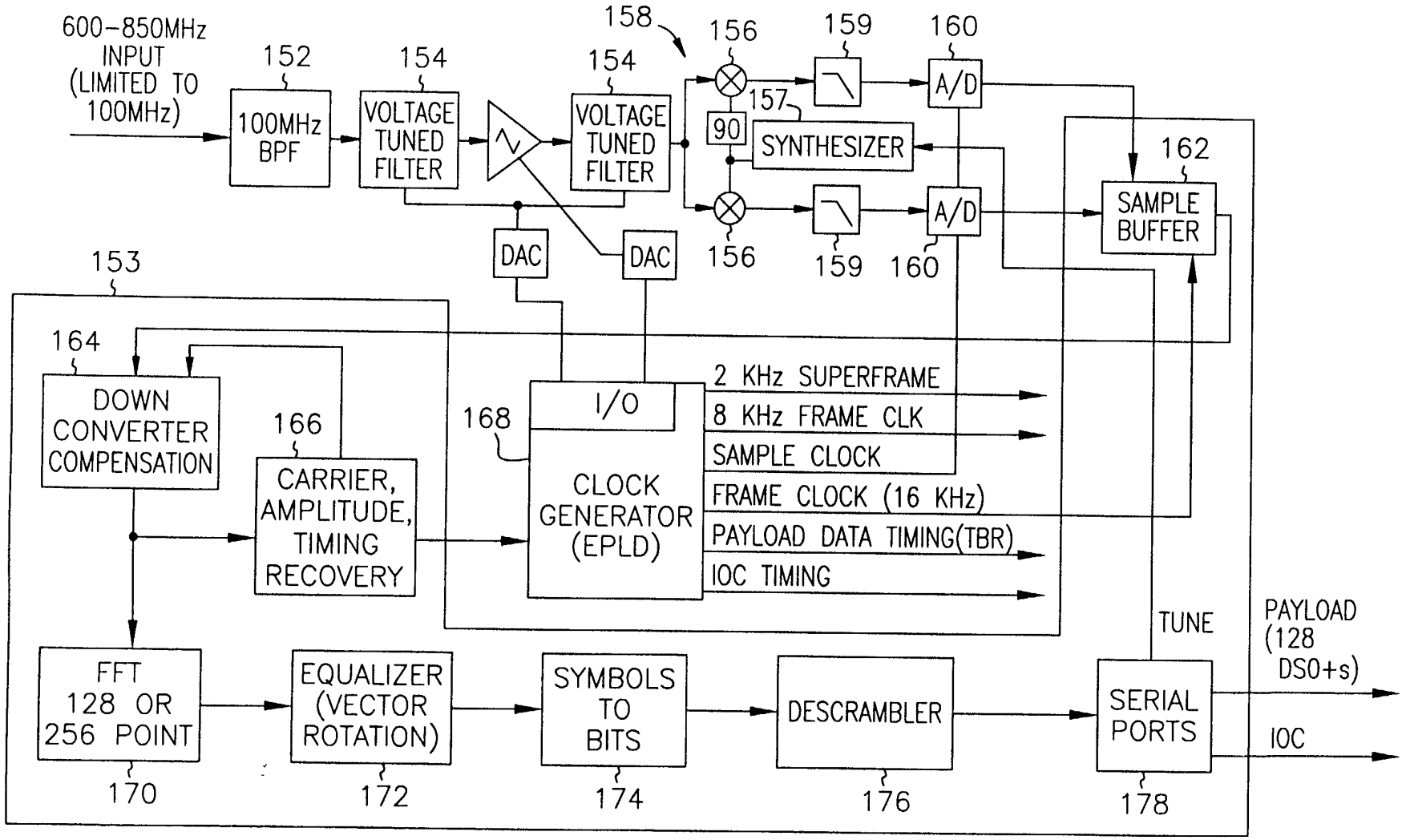

600-850MHz
INPUT
(LIMITED TO
100MHz)
152
100MHz
BPF
154
VOLTAGE
TUNED
FILTER
154
VOLTAGE
TUNED
FILTER
158
156
159
160
A/D
157
90
SYNTHESIZER
162
SAMPLE
BUFFER
A/D
156
159
160
DAC
DAC
153
164
DOWN
CONVERTER
COMPENSATION
166
CARRIER,
AMPLITUDE,
TIMING
RECOVERY
168
I/O
CLOCK
GENERATOR
(EPLD)
2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING
TUNE
PAYLOAD
(128
DS0+s)
IOC
FFT
128 OR
256 POINT
170
EQUALIZER
(VECTOR
ROTATION)
172
SYMBOLS
TO
BITS
174
DESCRAMBLER
176
SERIAL
PORTS
178

FIG. 22

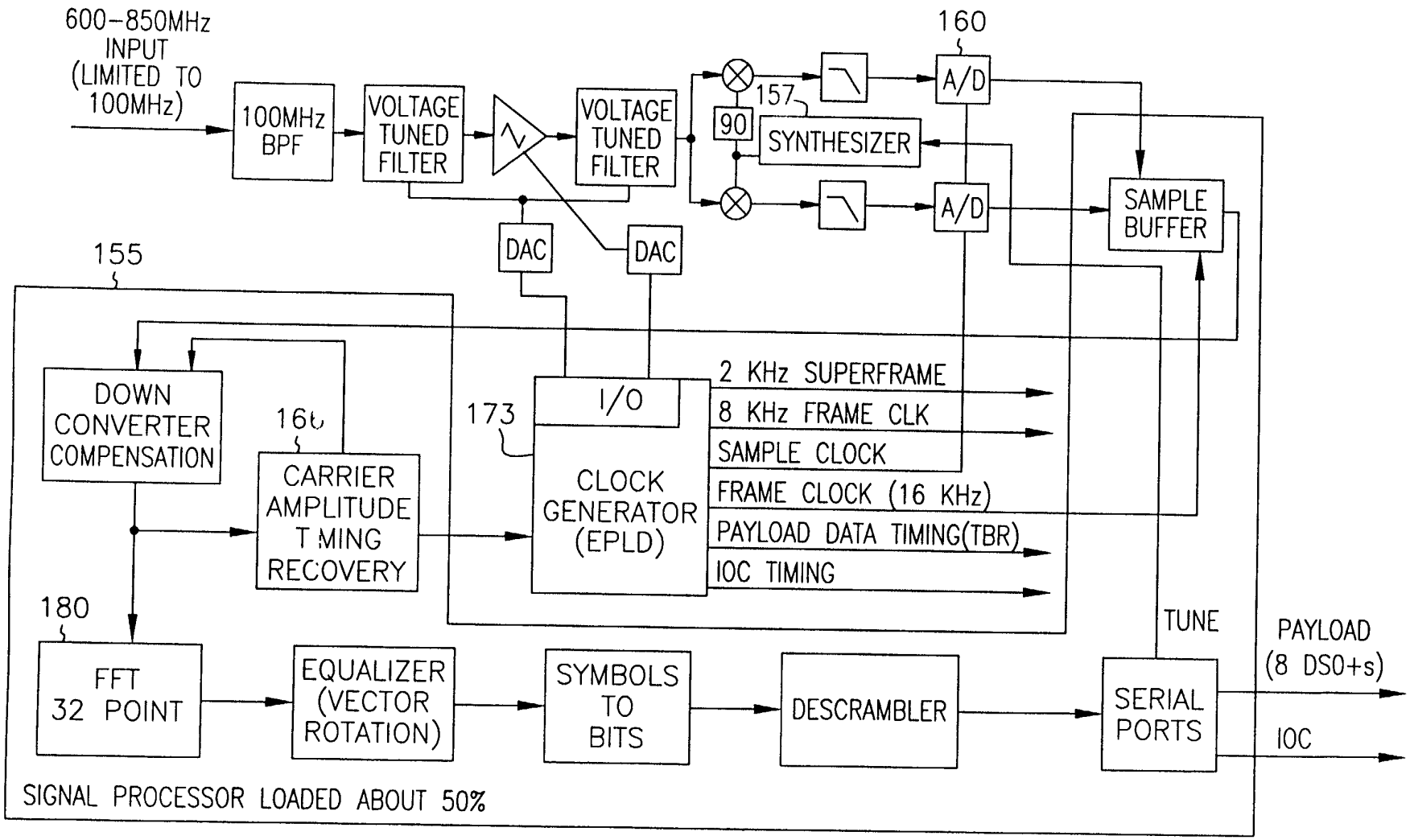

600-850MHz
INPUT
(LIMITED TO
100MHz)
100MHz
BPF
VOLTAGE
TUNED
FILTER
VOLTAGE
TUNED
FILTER
90
157
SYNTHESIZER
160
A/D
A/D
SAMPLE
BUFFER
DAC
DAC
155
DOWN
CONVERTER
COMPENSATION
161
CARRIER
AMPLITUDE
TIMING
RECOVERY
173
I/O
CLOCK
GENERATOR
(EPLD)
2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING
180
FFT
32 POINT
EQUALIZER
(VECTOR
ROTATION)
SYMBOLS
TO
BITS
DESCRAMBLER
TUNE
SERIAL
PORTS
PAYLOAD
(8 DS0+s)
IOC
SIGNAL PROCESSOR LOADED ABOUT 50%

FIG. 23

TD6020 "2ET060

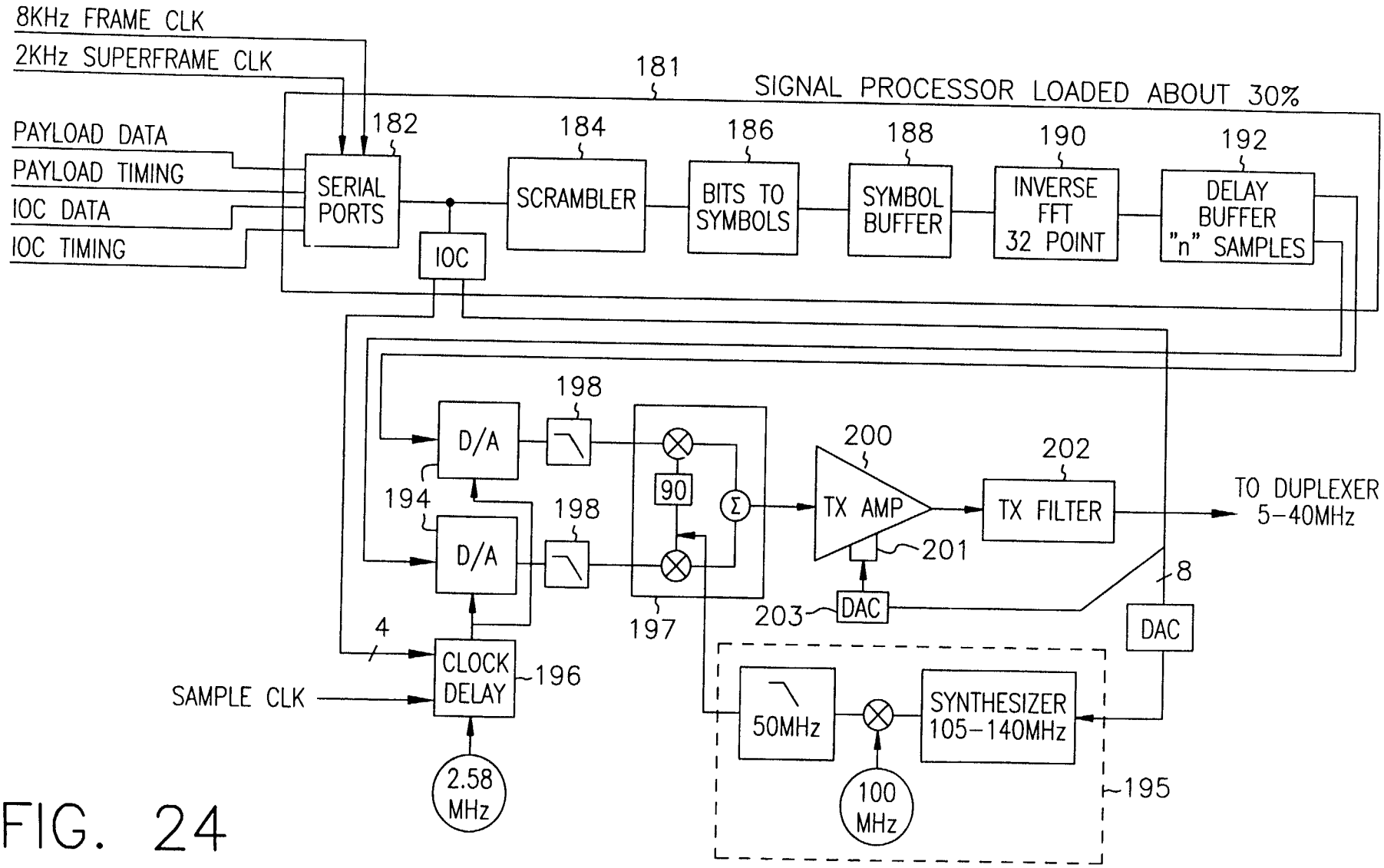


FIG. 24

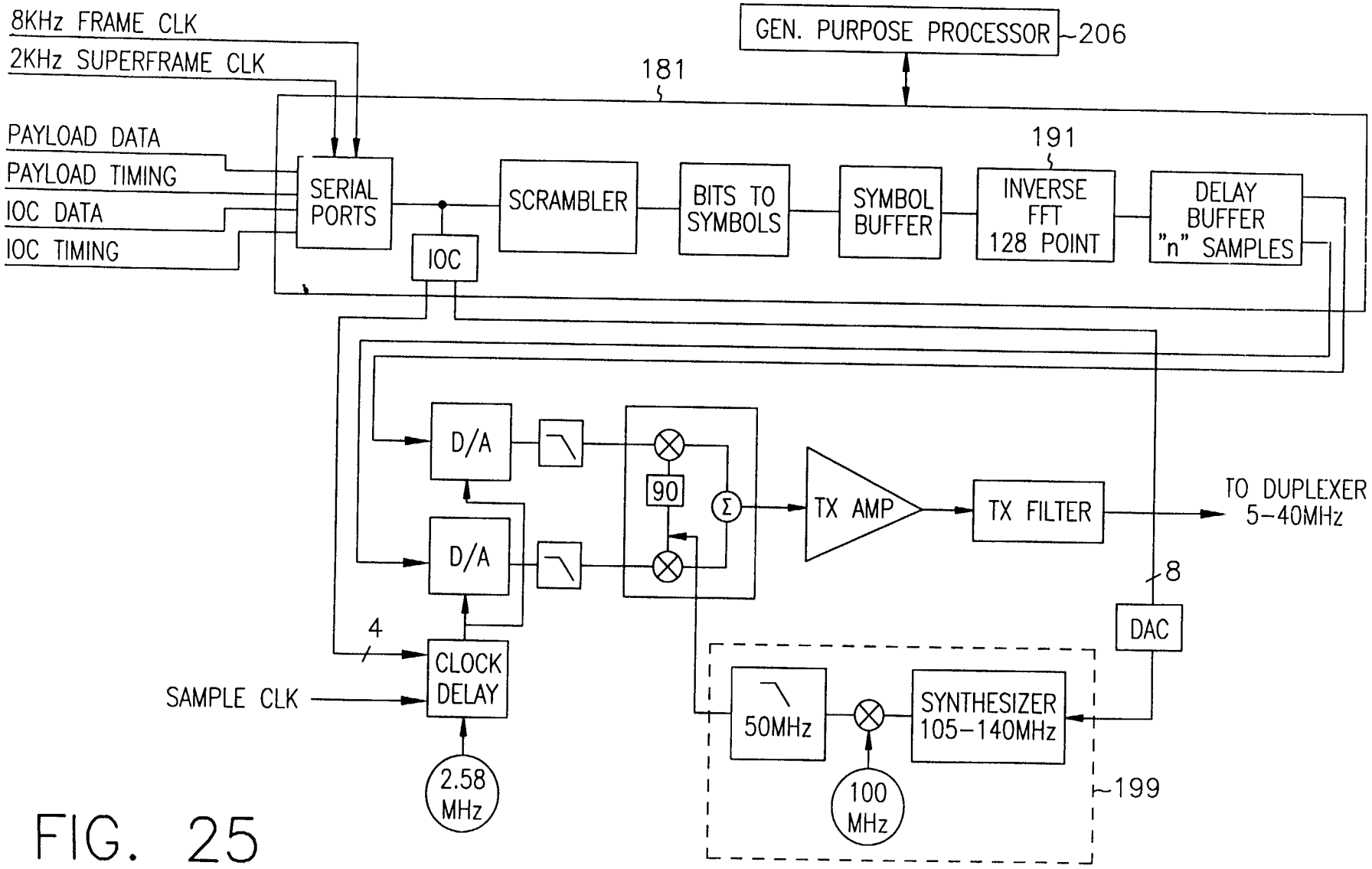

8KHz FRAME CLK
2KHz SUPERFRAME CLK
PAYLOAD DATA
PAYLOAD TIMING
IOC DATA
IOC TIMING
SERIAL PORTS
IOC
SCRAMBLER
BITS TO SYMBOLS
SYMBOL BUFFER
INVERSE FFT 128 POINT
DELAY BUFFER "n" SAMPLES
GEN. PURPOSE PROCESSOR
206
181
191
D/A
D/A
90
Σ
TX AMP
TX FILTER
TO DUPLEXER 5-40MHz
8
DAC
4
CLOCK DELAY
SAMPLE CLK
2.58 MHz
50MHz
100 MHz
SYNTHESIZER 105-140MHz
199

FIG. 25

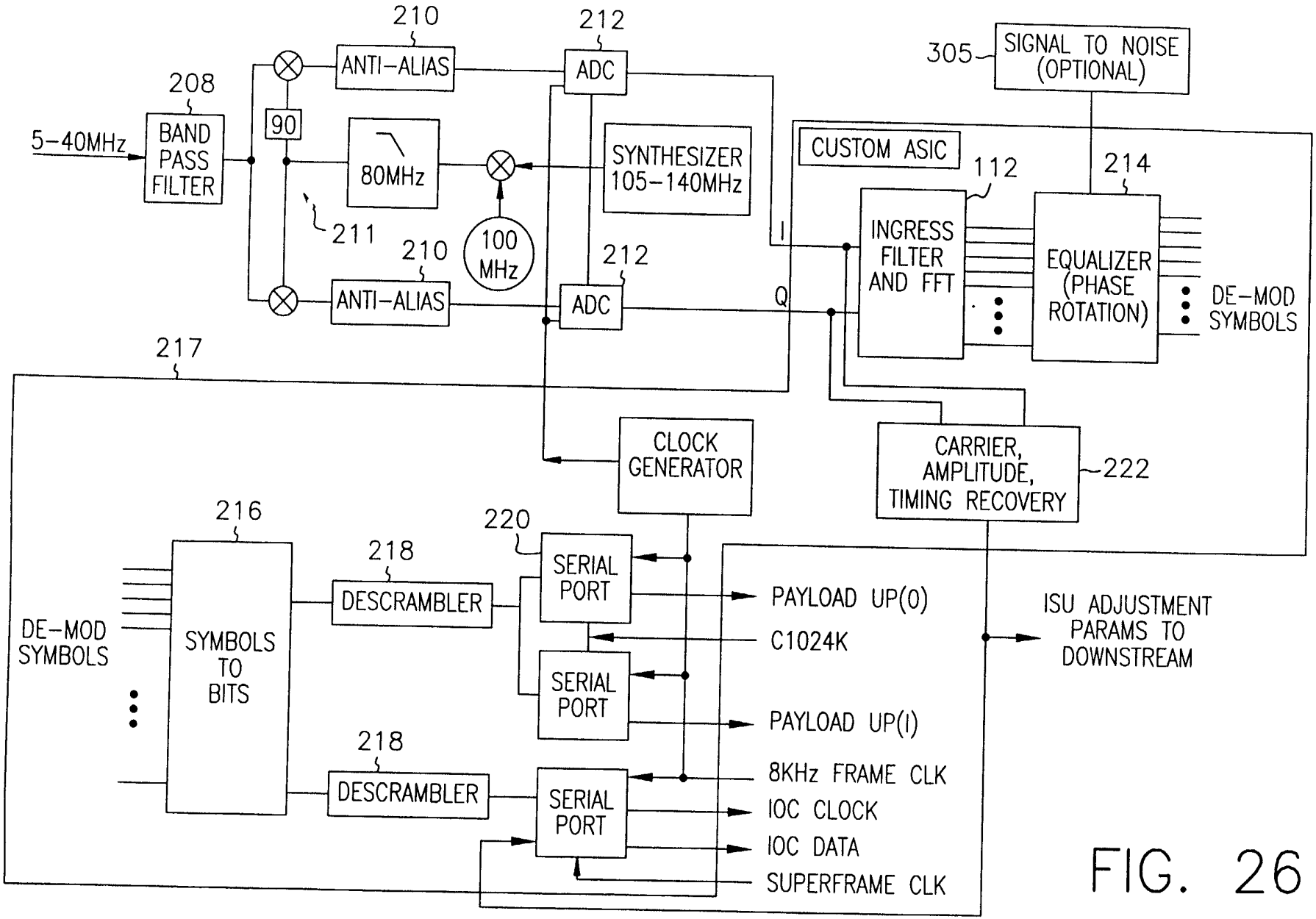

210
212
ANTI-ALIAS
ADC
208
BAND PASS FILTER
5-40MHz
90
80MHz
SYNTHESIZER 105-140MHz
211
100 MHz
210
212
ANTI-ALIAS
ADC
I
Q
305
SIGNAL TO NOISE (OPTIONAL)
CUSTOM ASIC
112
214
INGRESS FILTER AND FFT
EQUALIZER (PHASE ROTATION)
DE-MOD SYMBOLS
217
CLOCK GENERATOR
CARRIER, AMPLITUDE, TIMING RECOVERY
222
216
220
218
SERIAL PORT
DESCRAMBLER
PAYLOAD UP(0)
C1024K
DE-MOD SYMBOLS
SYMBOLS TO BITS
SERIAL PORT
PAYLOAD UP(I)
218
8KHz FRAME CLK
DESCRAMBLER
SERIAL PORT
IOC CLOCK
IOC DATA
SUPERFRAME CLK
ISU ADJUSTMENT PARAMS TO DOWNSTREAM

FIG. 26

5,859,852 4,359,750

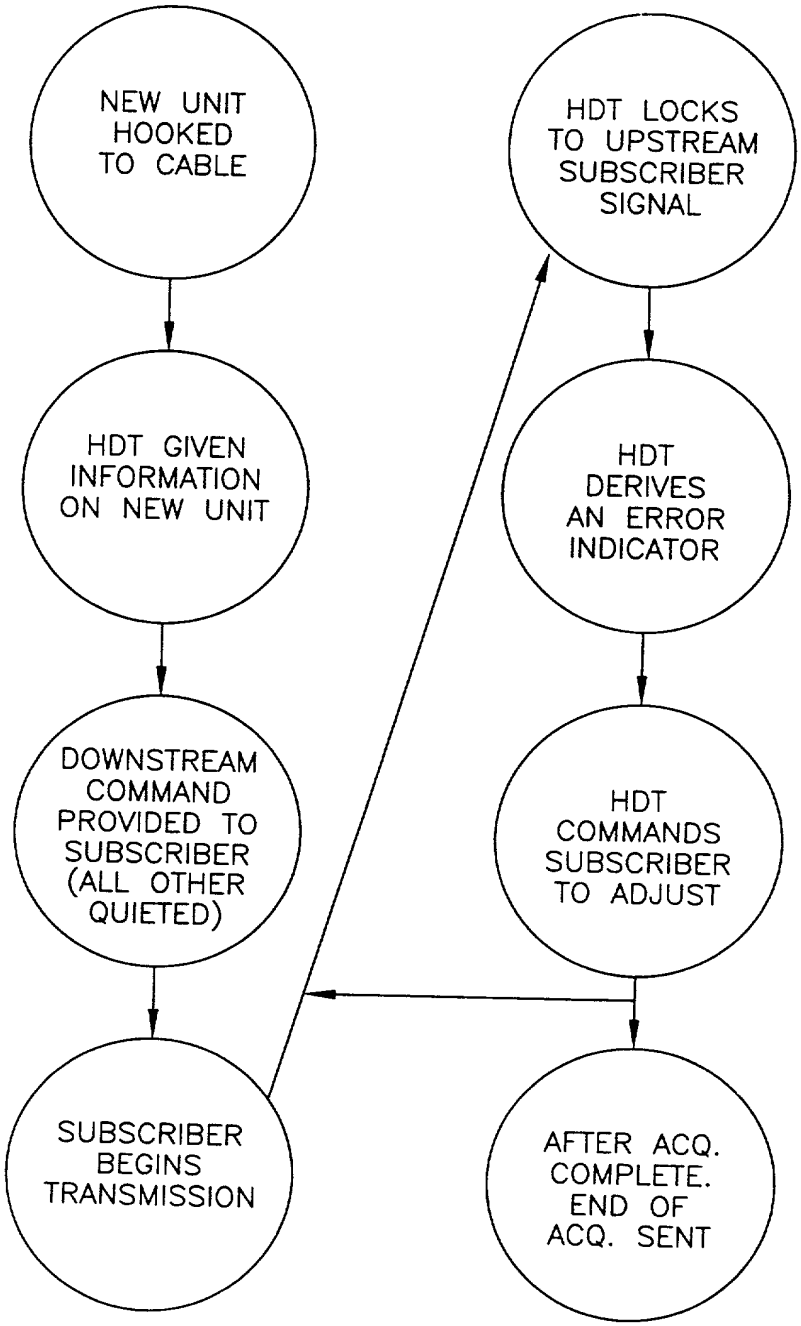


FIG. 27

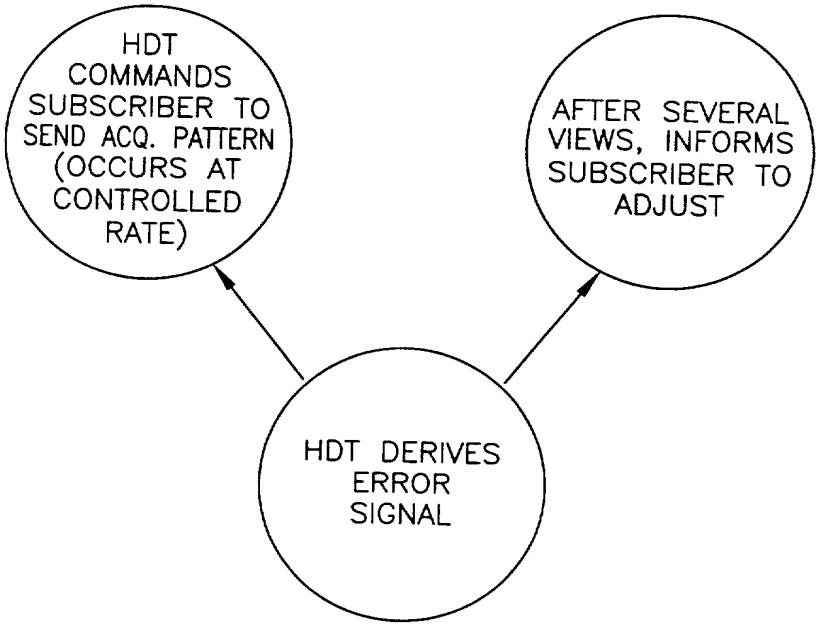

HDT COMMANDS SUBSCRIBER TO SEND ACQ. PATTERN (OCCURS AT CONTROLLED RATE)
AFTER SEVERAL VIEWS, INFORMS SUBSCRIBER TO ADJUST
HDT DERIVES ERROR SIGNAL

FIG. 28

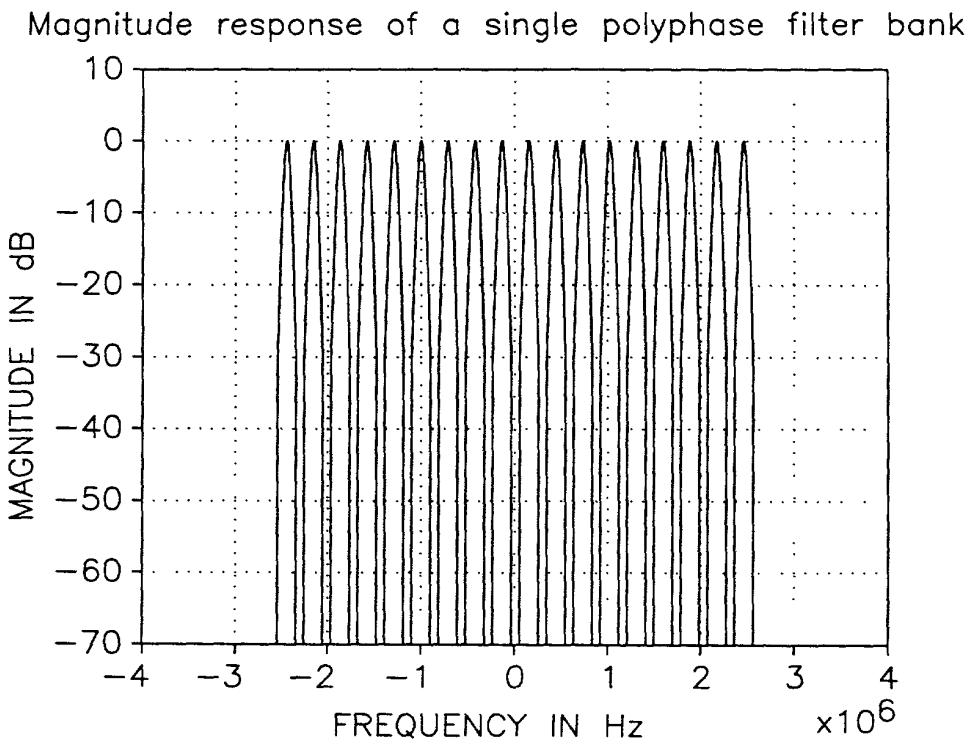

Magnitude response of a single polyphase filter bank
10
0
−10
−20
−30
−40
−50
−60
−70
MAGNITUDE IN dB
−4
−3
−2
−1
0
1
2
3
4
FREQUENCY IN Hz
x10^6

FIG. 29

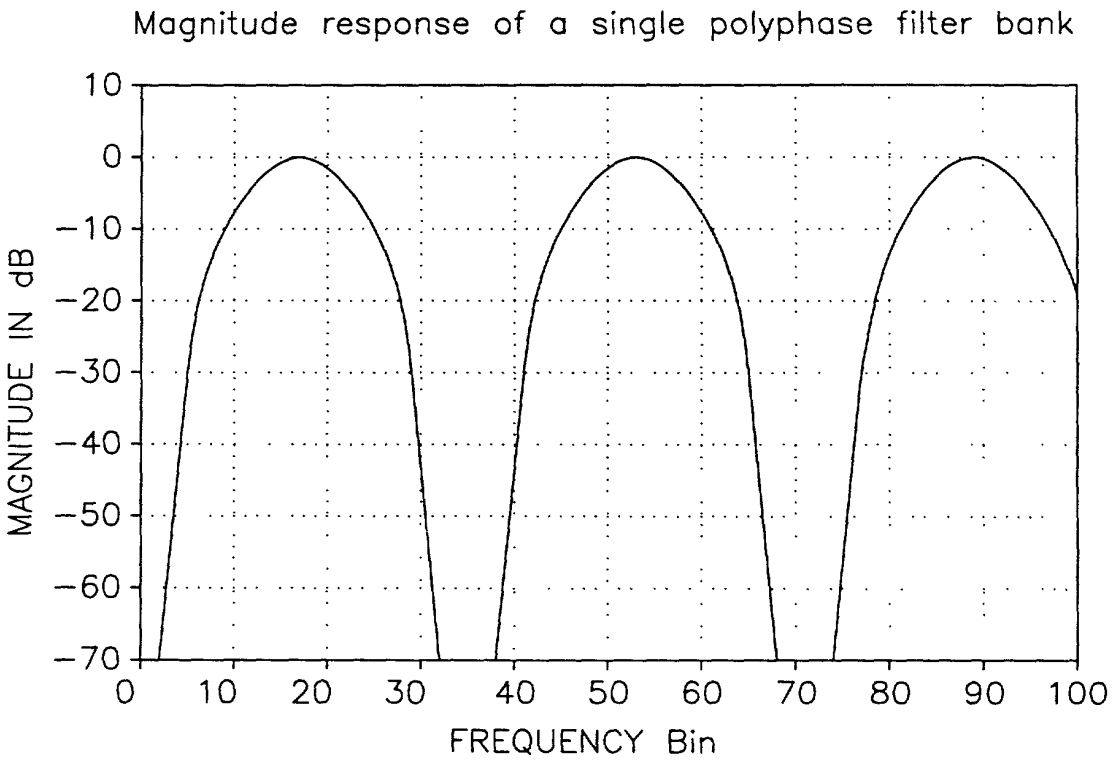

Magnitude response of a single polyphase filter bank
MAGNITUDE IN dB
10
0
−10
−20
−30
−40
−50
−60
−70
0
10
20
30
40
50
60
70
80
90
100
FREQUENCY Bin

FIG. 30

EP 0 660 570 A2

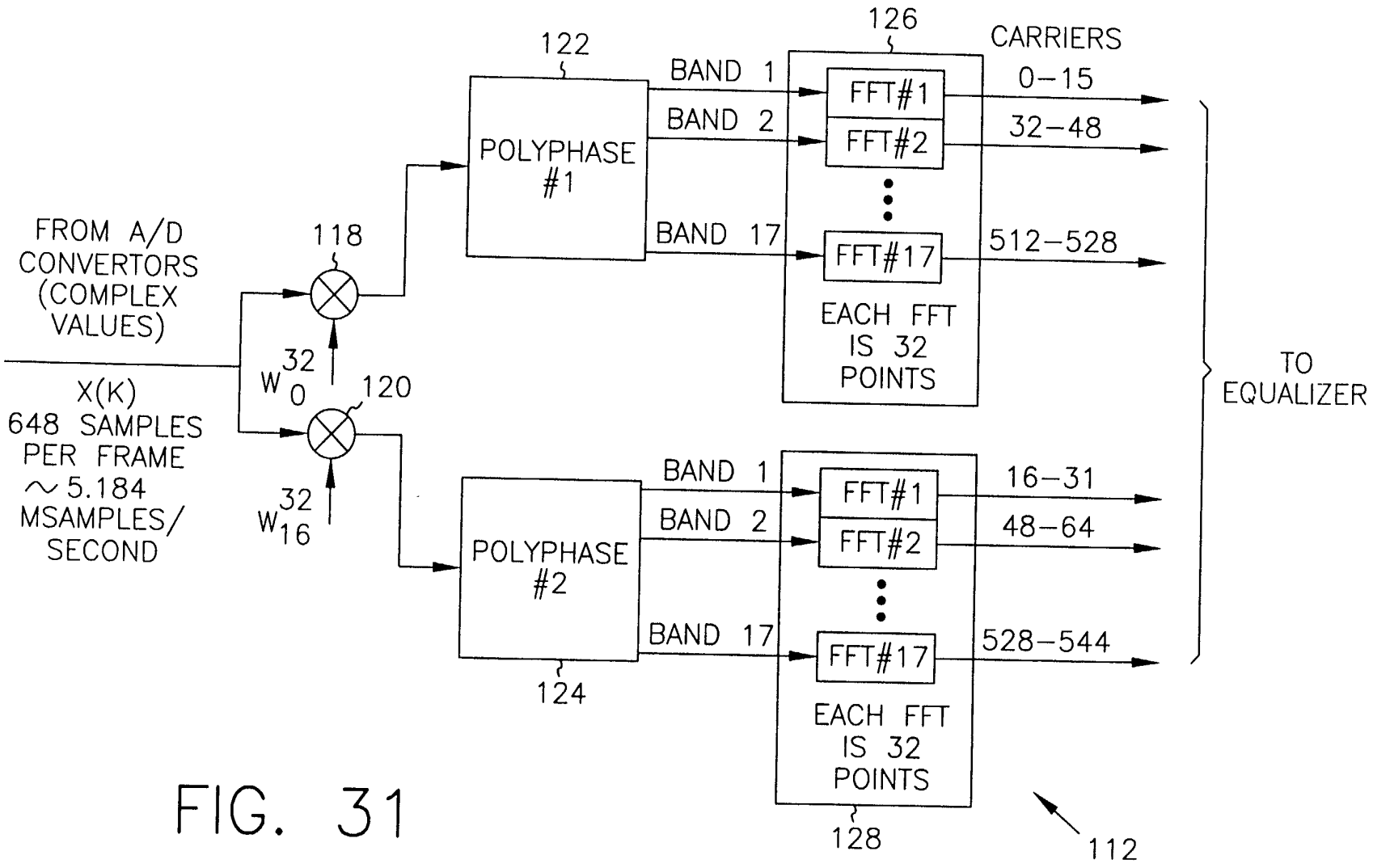


FIG. 31

T06020 "h2ET0660

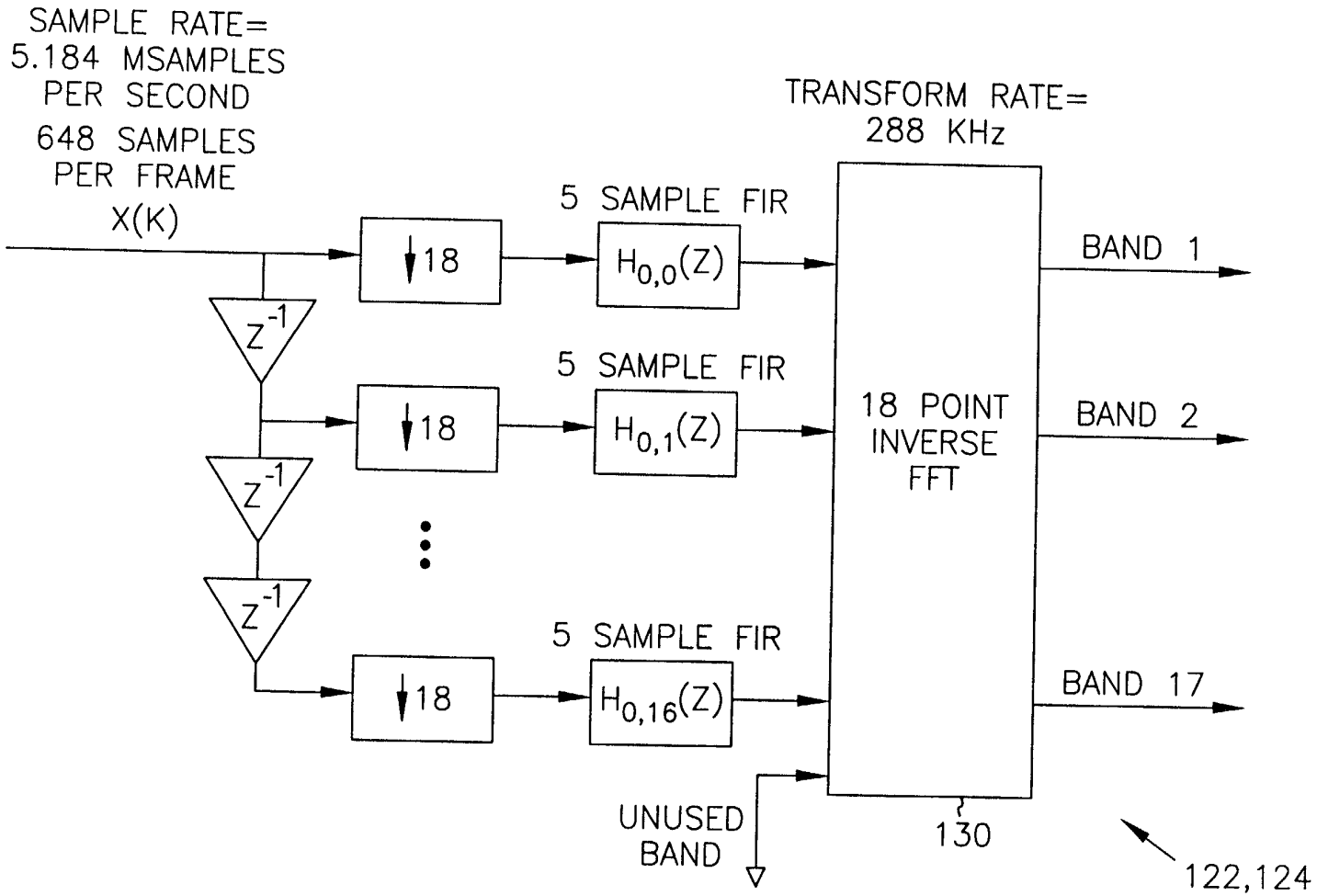


FIG. 32

FIG. 33

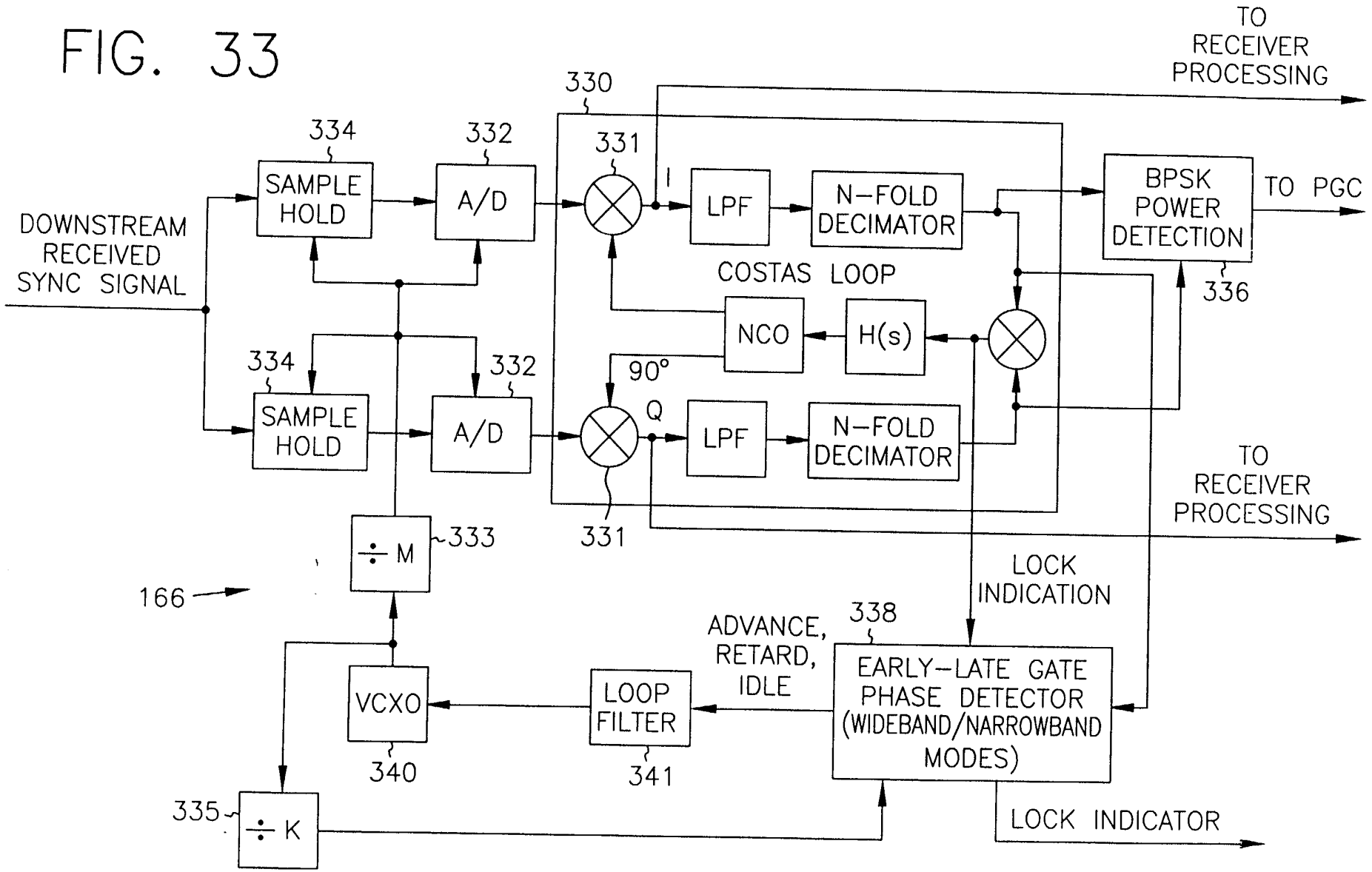
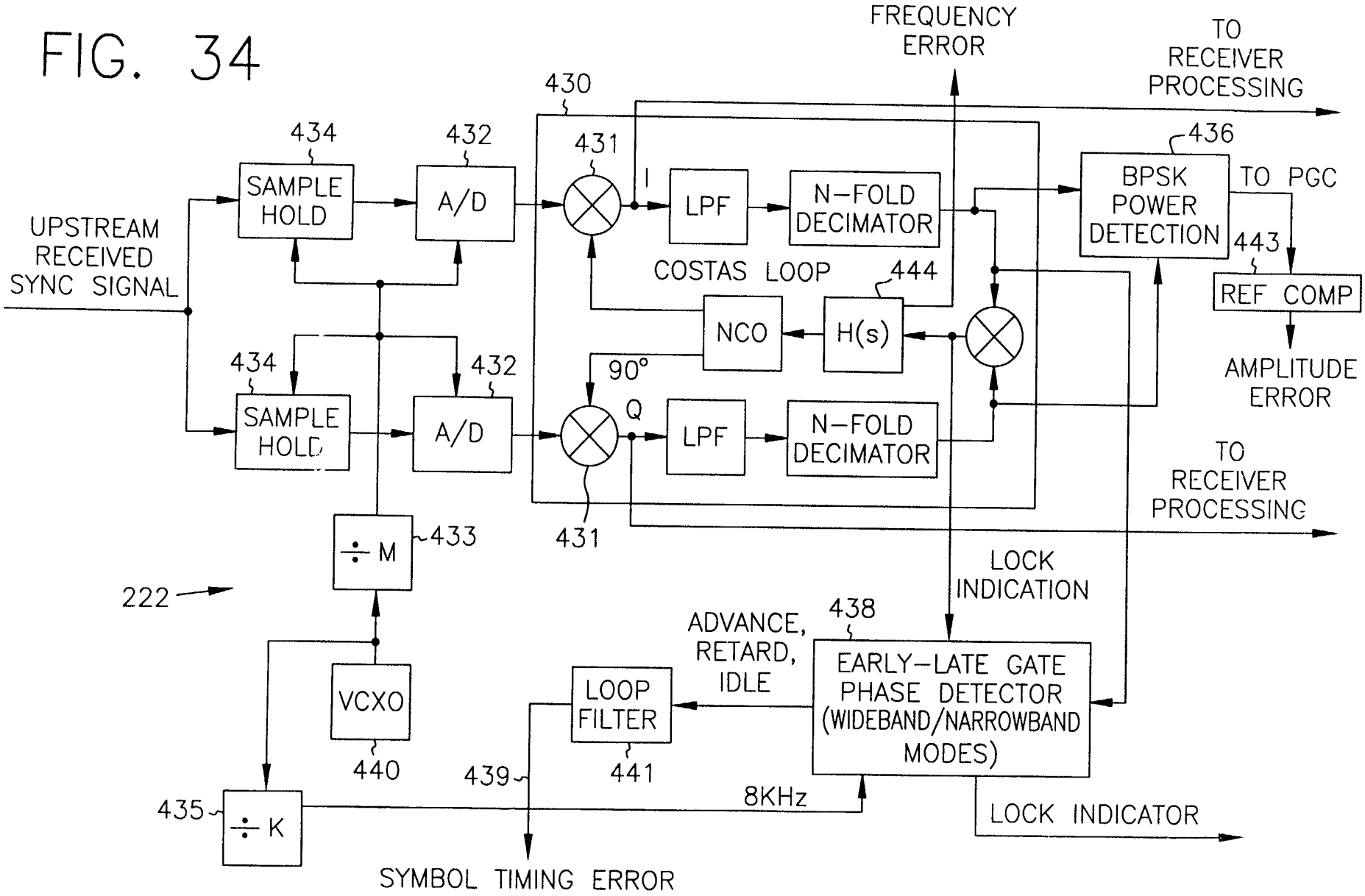

TO RECEIVER PROCESSING
330
334
332
331
SAMPLE HOLD
A/D
I
LPF
N-FOLD DECIMATOR
BPSK POWER DETECTION
TO PGC
DOWNSTREAM RECEIVED SYNC SIGNAL
COSTAS LOOP
NCO
H(s)
336
334
332
90°
SAMPLE HOLD
A/D
Q
LPF
N-FOLD DECIMATOR
TO RECEIVER PROCESSING
÷ M
333
331
166
LOCK INDICATION
338
ADVANCE, RETARD, IDLE
VCXO
LOOP FILTER
EARLY-LATE GATE PHASE DETECTOR (WIDEBAND/NARROWBAND MODES)
340
341
335
÷ K
LOCK INDICATOR

FIG. 34


FREQUENCY ERROR
TO RECEIVER PROCESSING
430
434
432
431
436
SAMPLE HOLD
A/D
I
LPF
N-FOLD DECIMATOR
BPSK POWER DETECTION
TO PGC
443
UPSTREAM RECEIVED SYNC SIGNAL
COSTAS LOOP
444
REF COMP
NCO
H(s)
AMPLITUDE ERROR
90°
Q
TO RECEIVER PROCESSING
÷ M
433
222
LOCK INDICATION
ADVANCE, RETARD, IDLE
438
VCXO
LOOP FILTER
EARLY-LATE GATE PHASE DETECTOR (WIDEBAND/NARROWBAND MODES)
440
439
441
8KHz
435
÷ K
LOCK INDICATOR
SYMBOL TIMING ERROR

T06020 "h2E70660

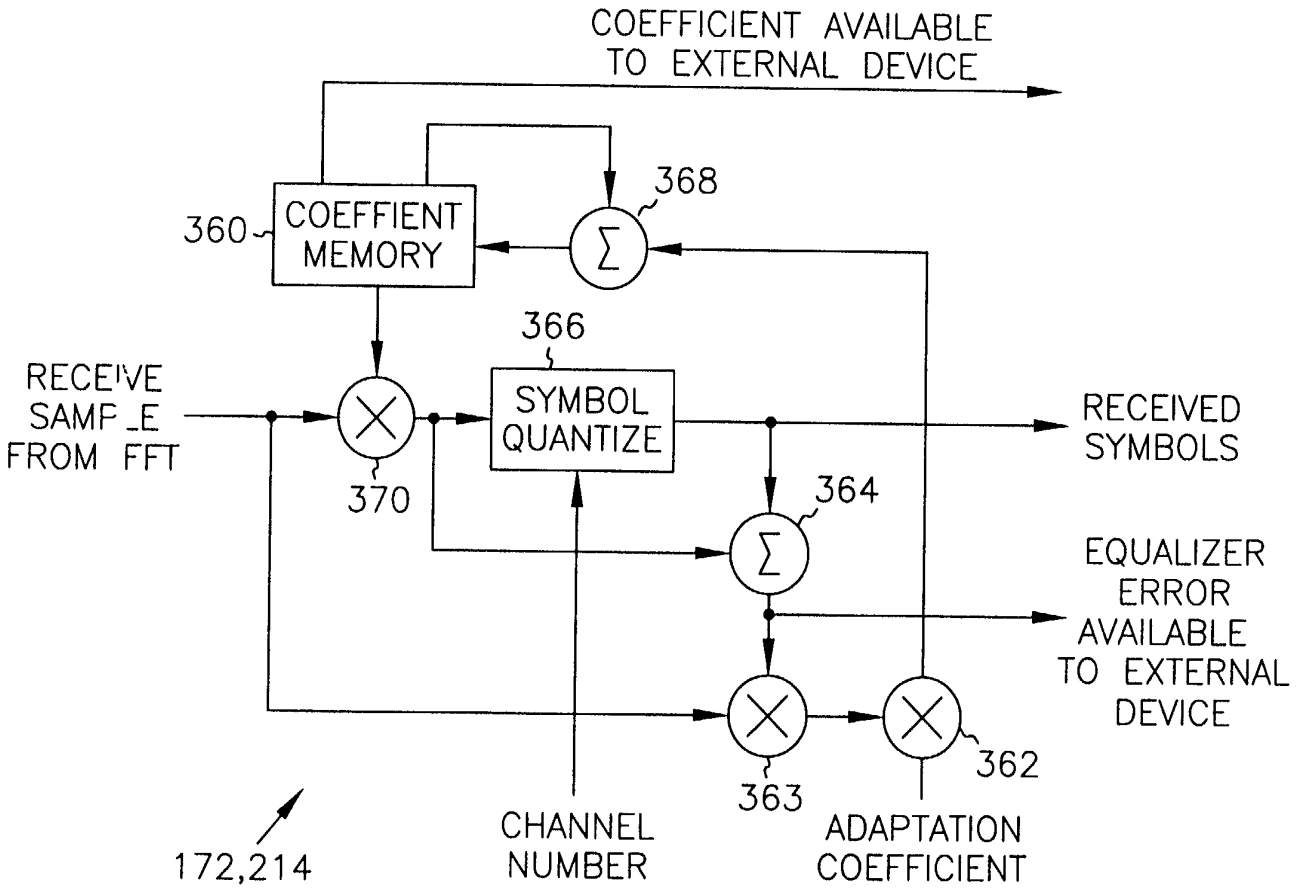


FIG. 35

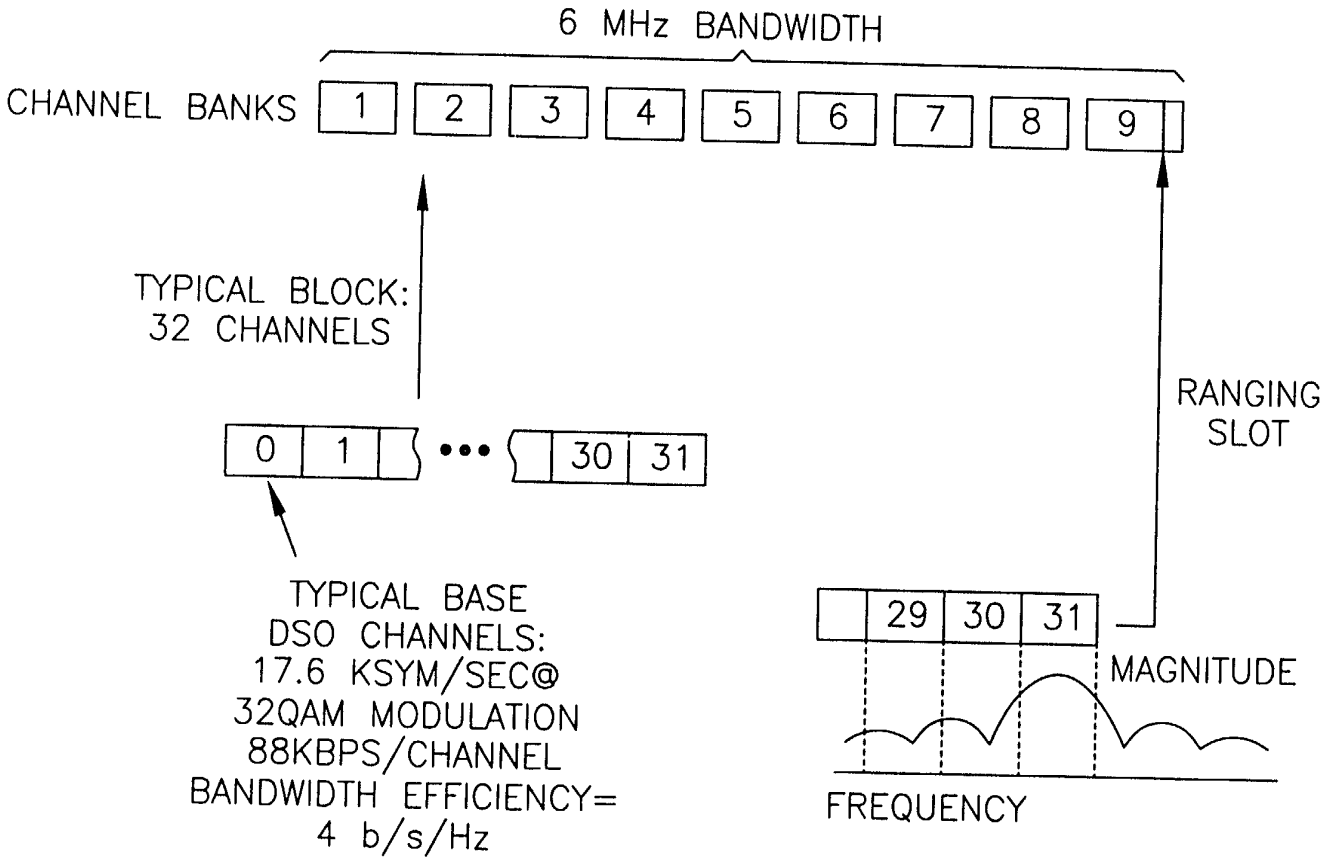

6 MHz BANDWIDTH
CHANNEL BANKS
1
2
3
4
5
6
7
8
9
TYPICAL BLOCK:
32 CHANNELS
0
1
30
31
RANGING
SLOT
TYPICAL BASE
DSO CHANNELS:
17.6 KSYM/SEC@
32QAM MODULATION
88KBPS/CHANNEL
BANDWIDTH EFFICIENCY=
4 b/s/Hz
29
30
31
MAGNITUDE
FREQUENCY

FIG. 36

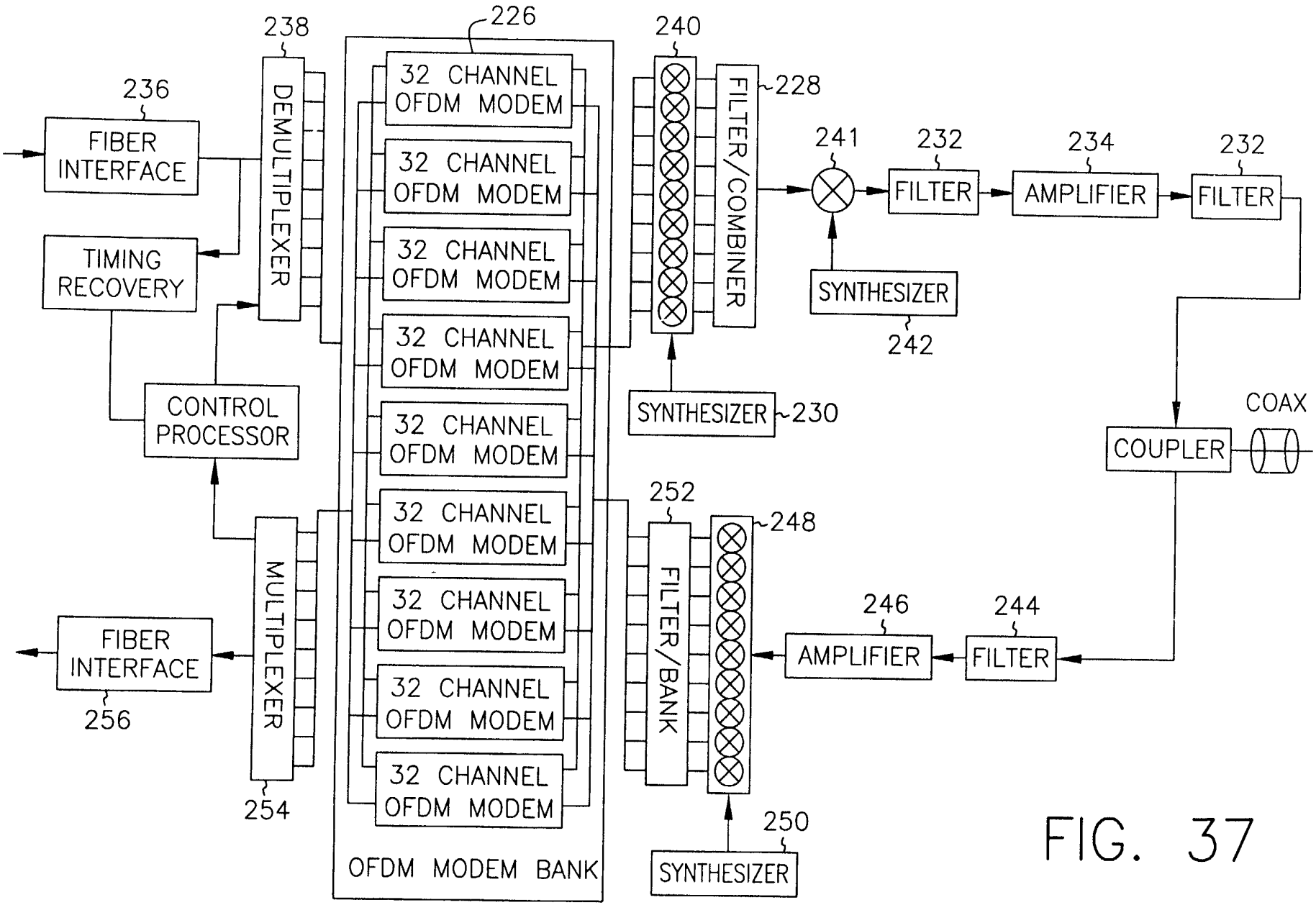

238
226
240
236
32 CHANNEL OFDM MODEM
FIBER INTERFACE
DEMULTIPLEXER
FILTER/COMBINER
228
241
232
234
232
FILTER
AMPLIFIER
FILTER
TIMING RECOVERY
SYNTHESIZER
242
CONTROL PROCESSOR
SYNTHESIZER
230
COAX
COUPLER
252
248
246
244
FILTER/BANK
AMPLIFIER
FILTER
FIBER INTERFACE
256
MULTIPLEXER
254
250
SYNTHESIZER
OFDM MODEM BANK

FIG. 37

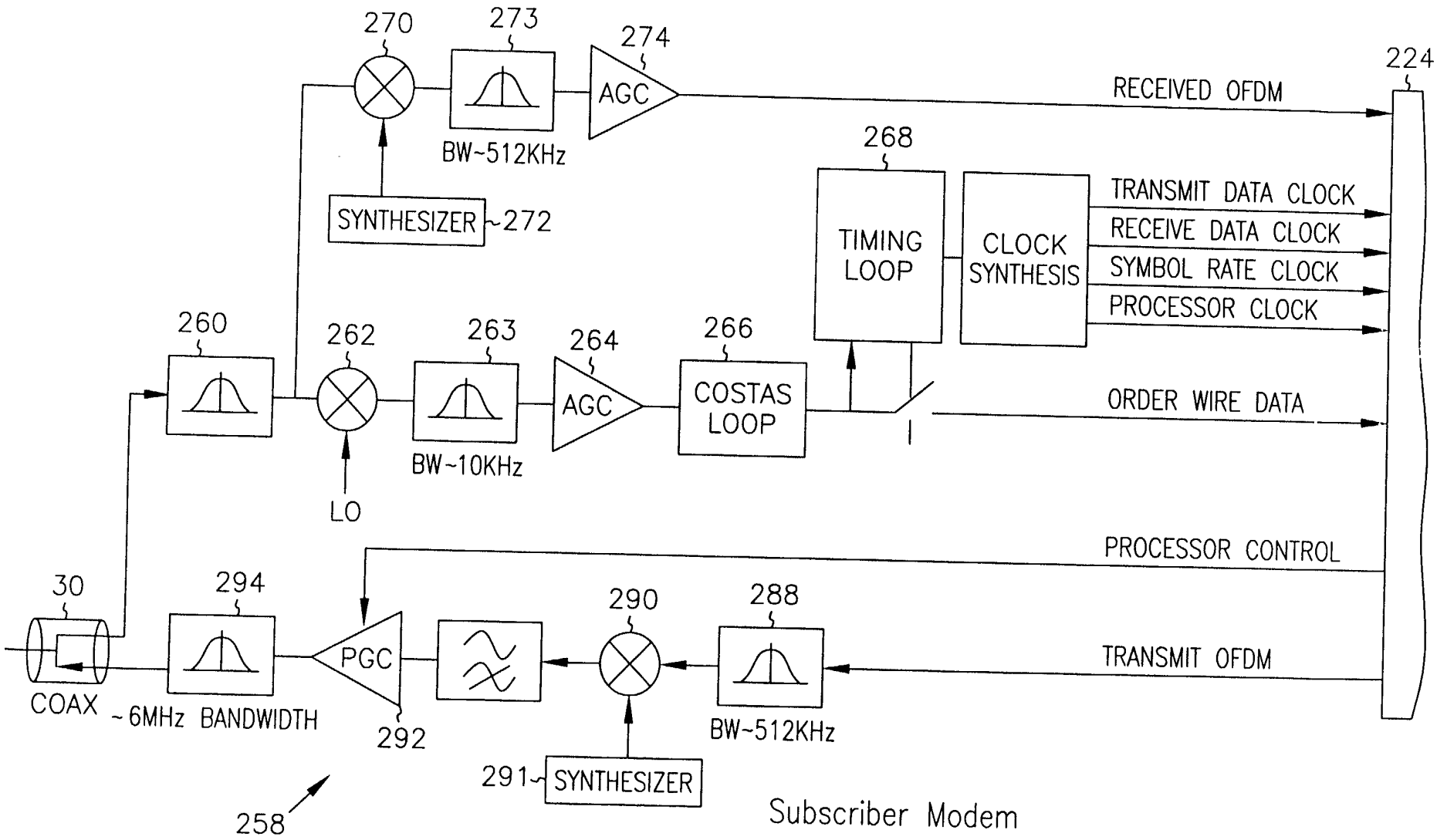

270
273
274
AGC
224
RECEIVED OFDM
BW~512KHz
268
SYNTHESIZER
272
TIMING LOOP
CLOCK SYNTHESIS
TRANSMIT DATA CLOCK
RECEIVE DATA CLOCK
SYMBOL RATE CLOCK
PROCESSOR CLOCK
260
262
263
264
266
AGC
COSTAS LOOP
ORDER WIRE DATA
BW~10KHz
LO
PROCESSOR CONTROL
30
294
290
288
PGC
TRANSMIT OFDM
COAX
~6MHz BANDWIDTH
292
BW~512KHz
291
SYNTHESIZER
258
Subscriber Modem

FIG. 38

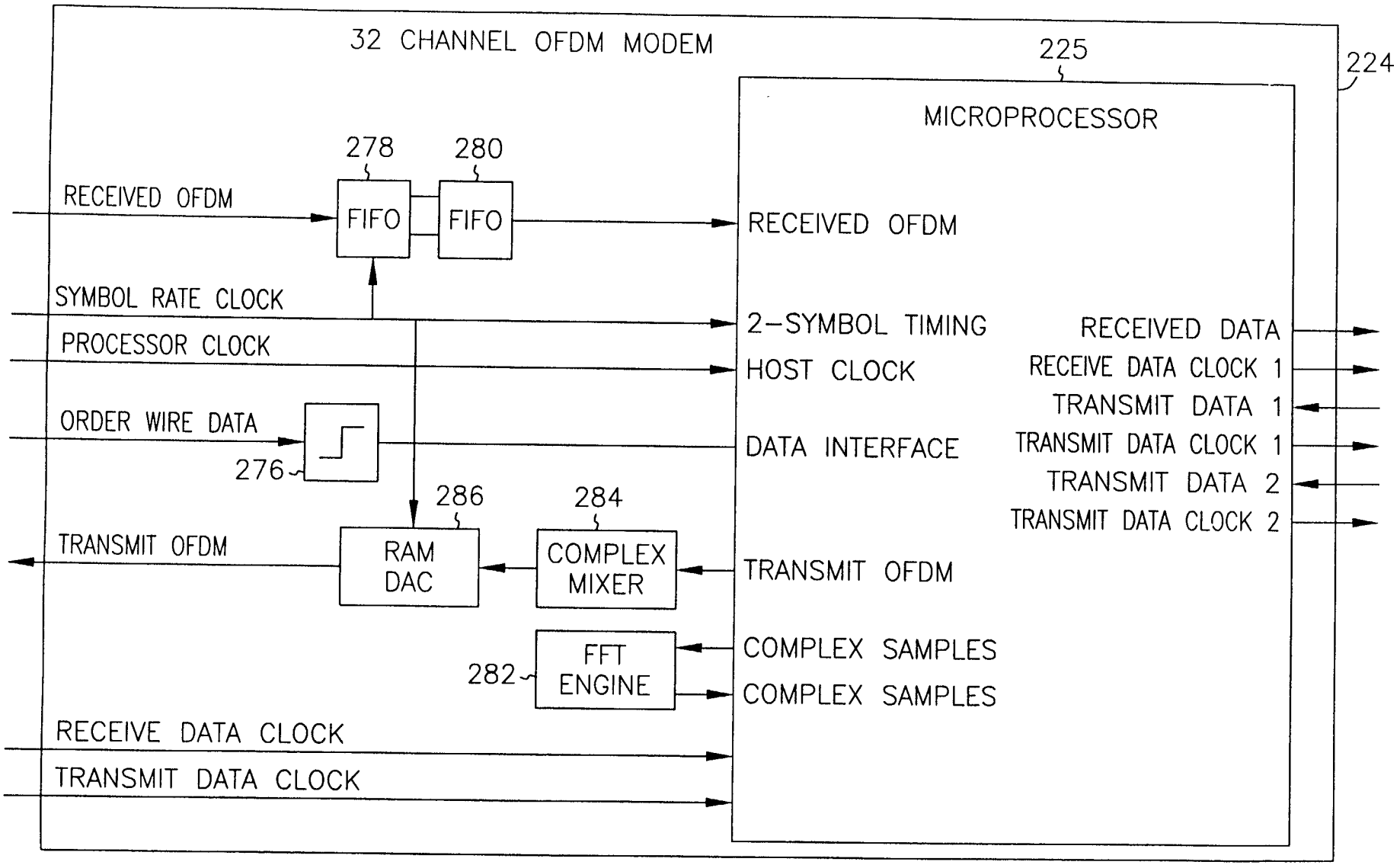

32 CHANNEL OFDM MODEM
225
224
MICROPROCESSOR
278
280
RECEIVED OFDM
FIFO
FIFO
RECEIVED OFDM
SYMBOL RATE CLOCK
2-SYMBOL TIMING
RECEIVED DATA
PROCESSOR CLOCK
HOST CLOCK
RECEIVE DATA CLOCK 1
TRANSMIT DATA 1
ORDER WIRE DATA
DATA INTERFACE
TRANSMIT DATA CLOCK 1
276
TRANSMIT DATA 2
286
284
TRANSMIT DATA CLOCK 2
TRANSMIT OFDM
RAM DAC
COMPLEX MIXER
TRANSMIT OFDM
COMPLEX SAMPLES
282
FFT ENGINE
COMPLEX SAMPLES
RECEIVE DATA CLOCK
TRANSMIT DATA CLOCK

FIG. 39

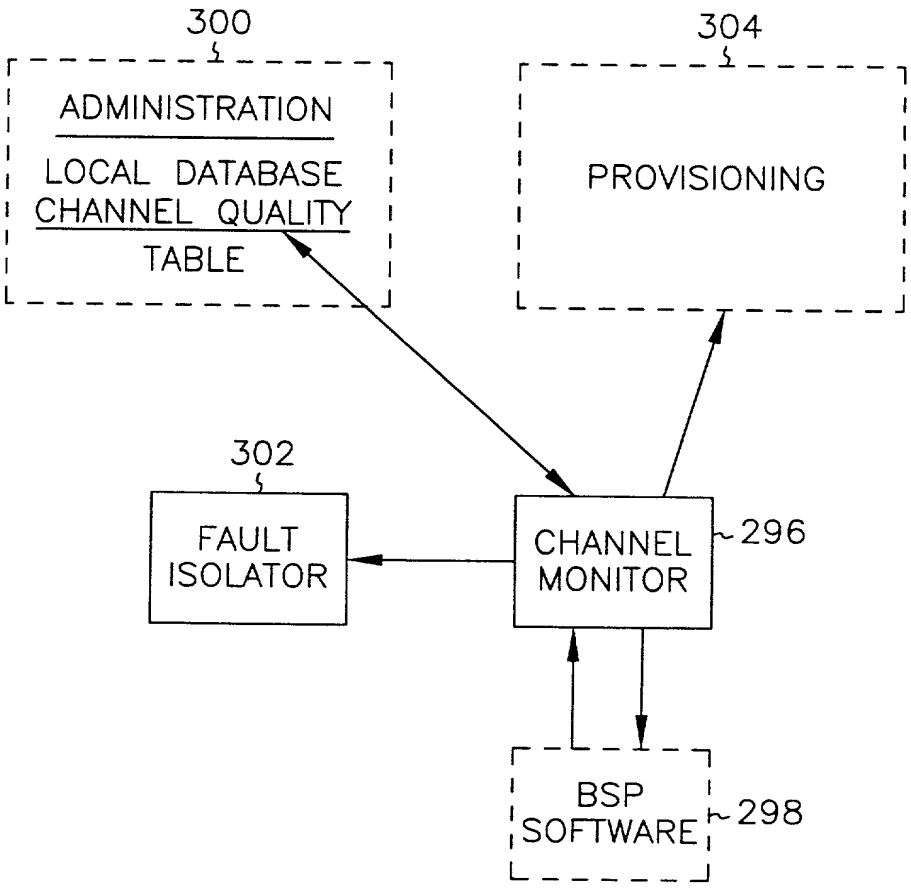

300
ADMINISTRATION
LOCAL DATABASE
CHANNEL QUALITY
TABLE
304
PROVISIONING
302
FAULT
ISOLATOR
CHANNEL
MONITOR
296
BSP
SOFTWARE
298

FIG. 40

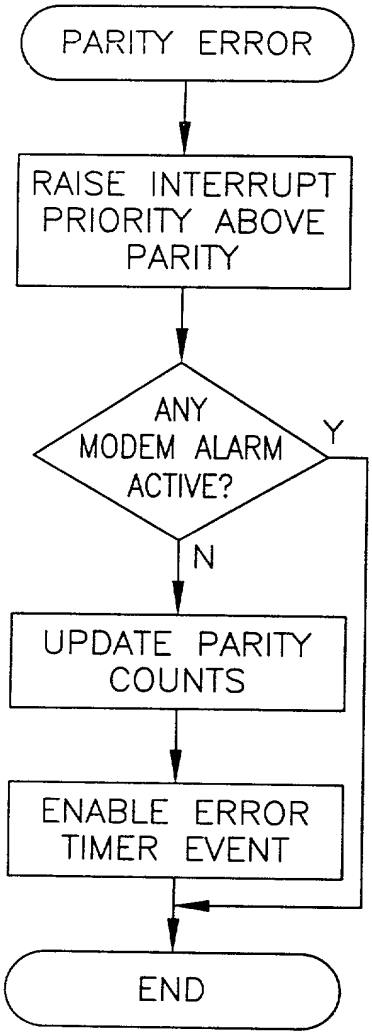


FIG. 41

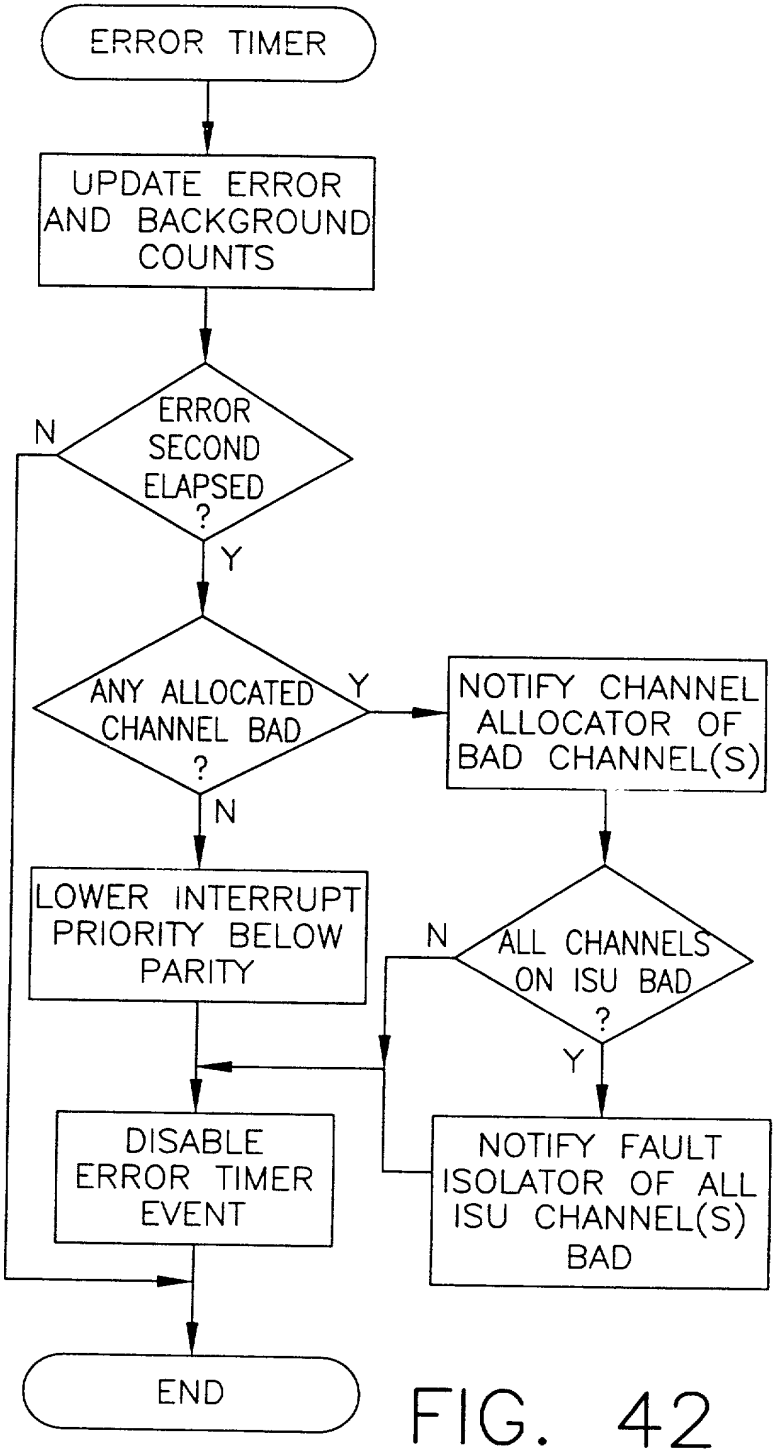


FIG. 42

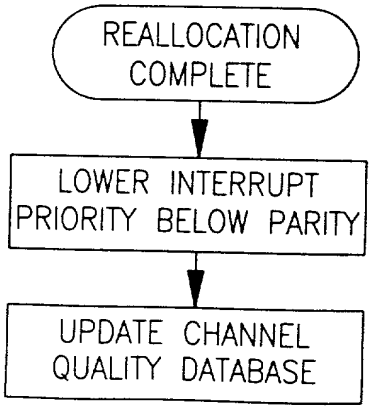
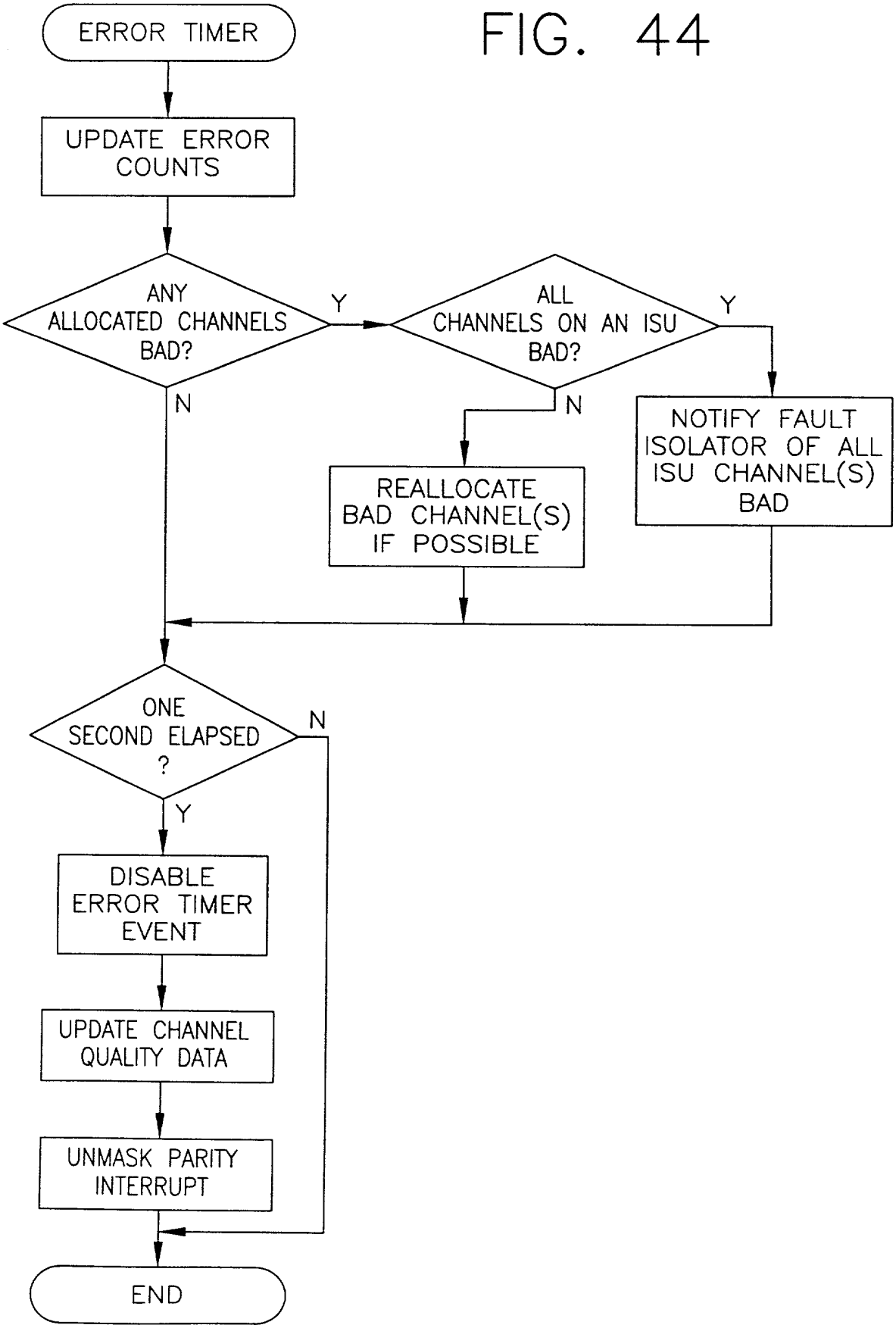


FIG. 43

FIG. 44


ERROR TIMER
UPDATE ERROR COUNTS
ANY ALLOCATED CHANNELS BAD?
Y
ALL CHANNELS ON AN ISU BAD?
Y
N
N
NOTIFY FAULT ISOLATOR OF ALL ISU CHANNEL(S) BAD
REALLOCATE BAD CHANNEL(S) IF POSSIBLE
ONE SECOND ELAPSED ?
N
Y
DISABLE ERROR TIMER EVENT
UPDATE CHANNEL QUALITY DATA
UNMASK PARITY INTERRUPT
END

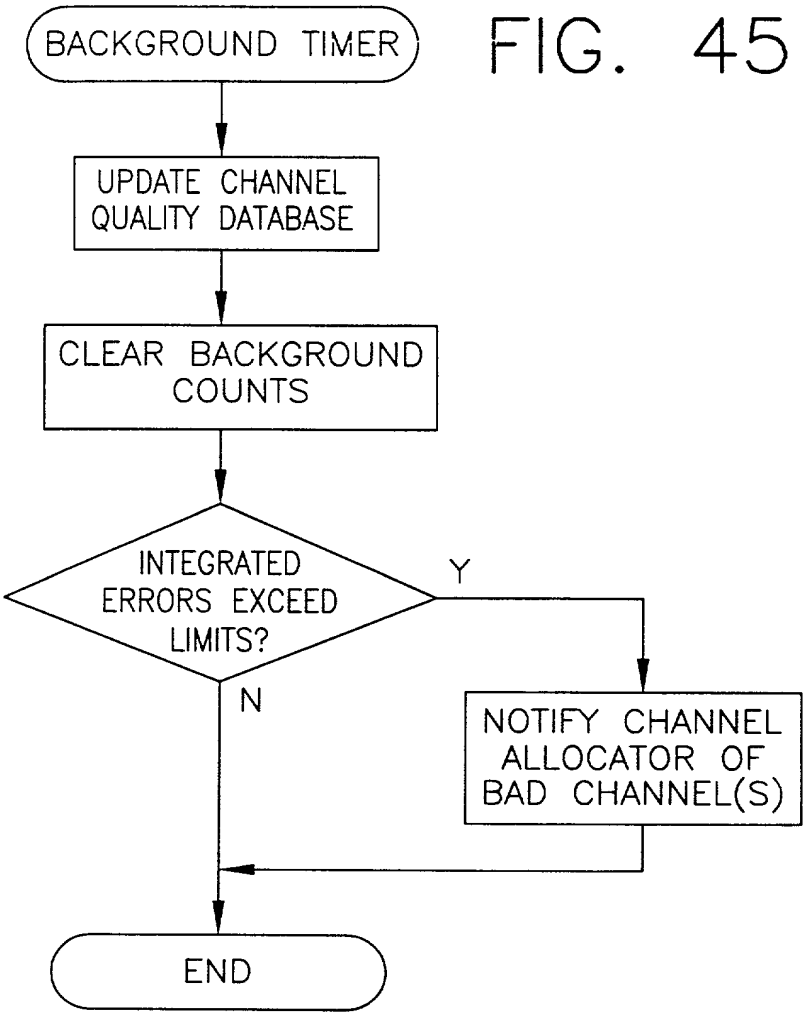

BACKGROUND TIMER
UPDATE CHANNEL QUALITY DATABASE
CLEAR BACKGROUND COUNTS
INTEGRATED ERRORS EXCEED LIMITS?
Y
N
NOTIFY CHANNEL ALLOCATOR OF BAD CHANNEL(S)
END

FIG. 45

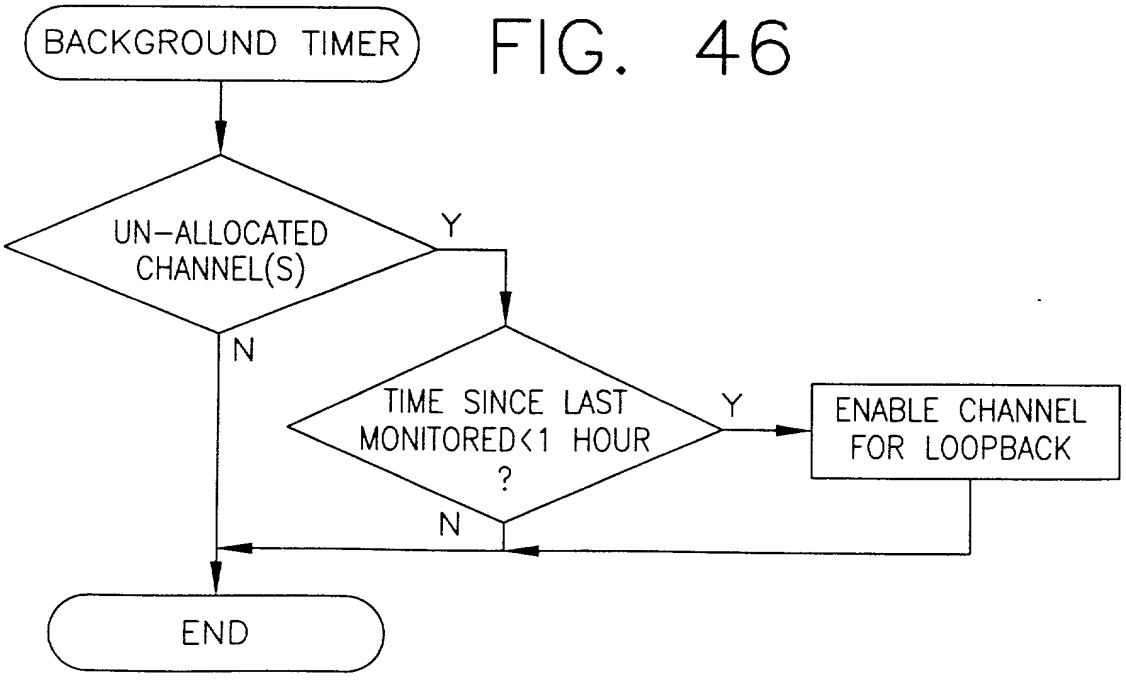

BACKGROUND TIMER
UN-ALLOCATED CHANNEL(S)
Y
N
TIME SINCE LAST MONITORED<1 HOUR ?
Y
N
ENABLE CHANNEL FOR LOOPBACK
END

FIG. 46

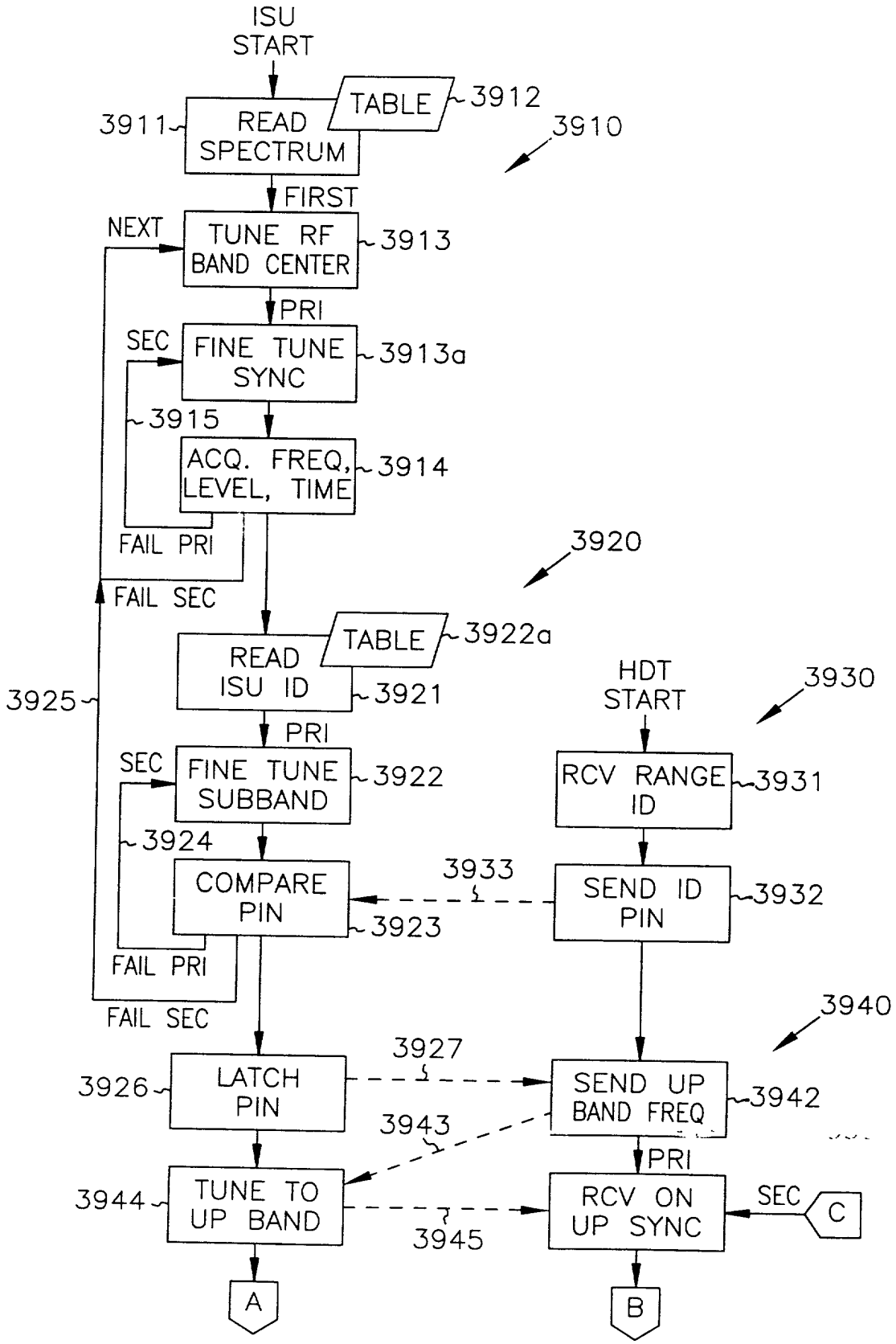

ISU START
TABLE
3912
3911
READ SPECTRUM
3910
FIRST
NEXT
TUNE RF BAND CENTER
3913
PRI
SEC
FINE TUNE SYNC
3913a
3915
ACQ. FREQ, LEVEL, TIME
3914
FAIL PRI
FAIL SEC
3920
TABLE
3922a
READ ISU ID
3921
3925
PRI
SEC
FINE TUNE SUBBAND
3922
3924
COMPARE PIN
3923
FAIL PRI
FAIL SEC
HDT START
3930
RCV RANGE ID
3931
3933
SEND ID PIN
3932
3940
3927
3926
LATCH PIN
SEND UP BAND FREQ
3942
3943
PRI
3944
TUNE TO UP BAND
RCV ON UP SYNC
SEC
C
3945
A
B

FIG. 47

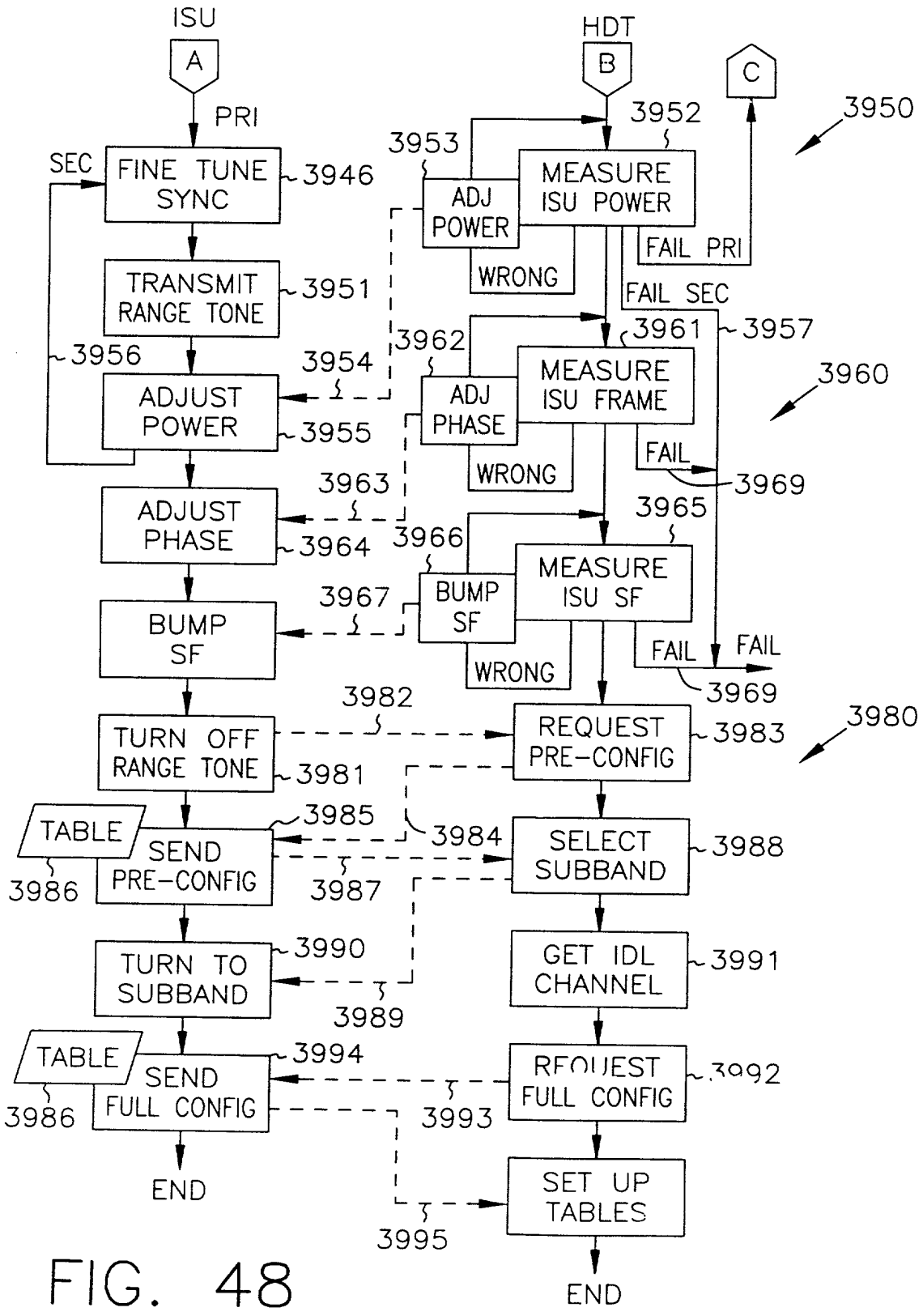

ISU
A
PRI
SEC
FINE TUNE SYNC
3946
TRANSMIT RANGE TONE
3951
3956
ADJUST POWER
3955
3954
ADJUST PHASE
3964
3963
BUMP SF
3967
TURN OFF RANGE TONE
3981
TABLE
SEND PRE-CONFIG
3986
3985
TURN TO SUBBAND
3990
3989
TABLE
SEND FULL CONFIG
3986
3994
END
HDT
B
C
3950
3952
3953
MEASURE ISU POWER
ADJ POWER
WRONG
FAIL PRI
FAIL SEC
3961
3957
3962
MEASURE ISU FRAME
ADJ PHASE
WRONG
FAIL
3969
3960
3965
3966
MEASURE ISU SF
BUMP SF
WRONG
FAIL
FAIL
3969
3982
REQUEST PRE-CONFIG
3983
3980
3984
SELECT SUBBAND
3988
3987
GET IDL CHANNEL
3991
REQUEST FULL CONFIG
3992
3993
SET UP TABLES
3995
END

FIG. 48

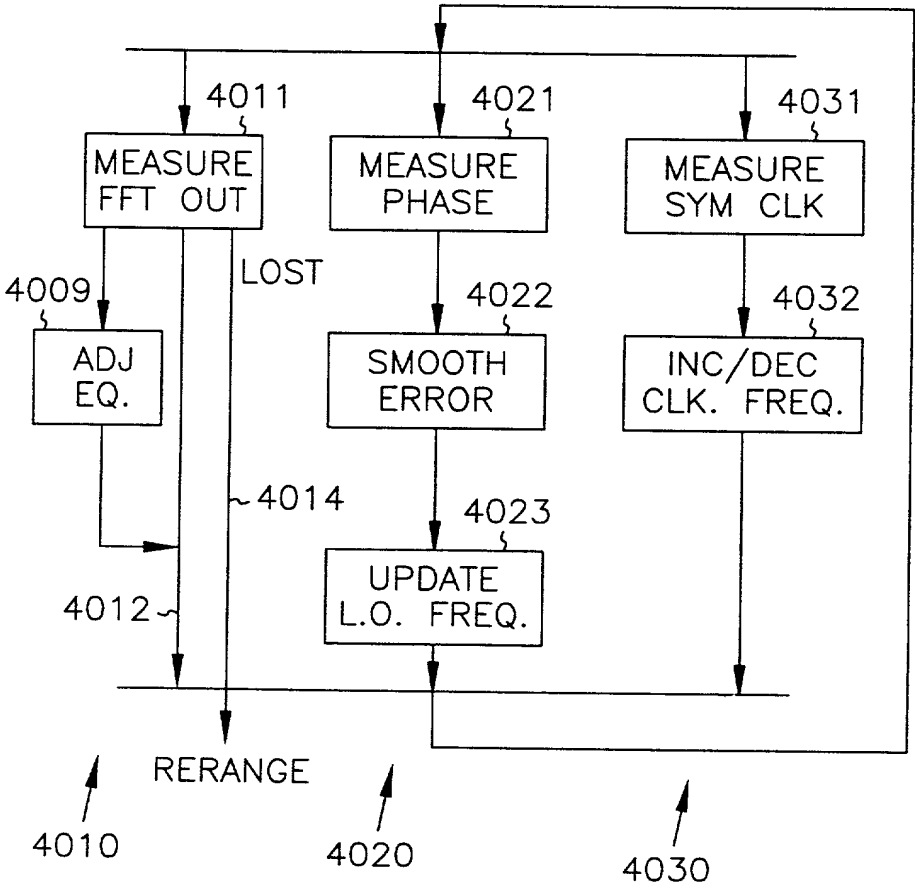

4011
4021
4031
MEASURE FFT OUT
MEASURE PHASE
MEASURE SYM CLK
LOST
4009
4022
4032
ADJ EQ.
SMOOTH ERROR
INC/DEC CLK. FREQ.
4014
4023
UPDATE L.O. FREQ.
4012
RERANGE
4010
4020
4030

FIG. 49

US 6,963,747 B2

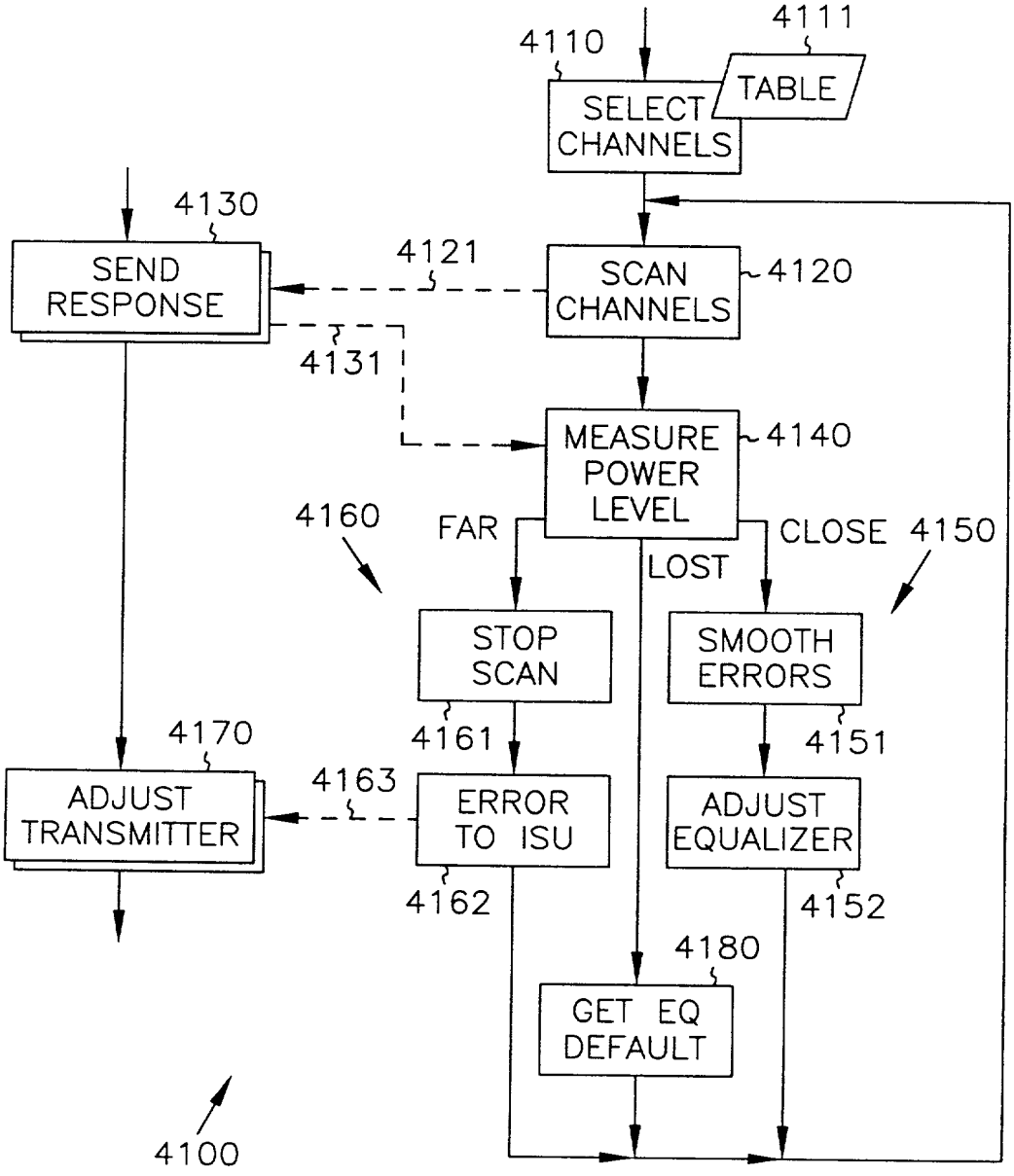


FIG. 50

T06020 "WO9839860

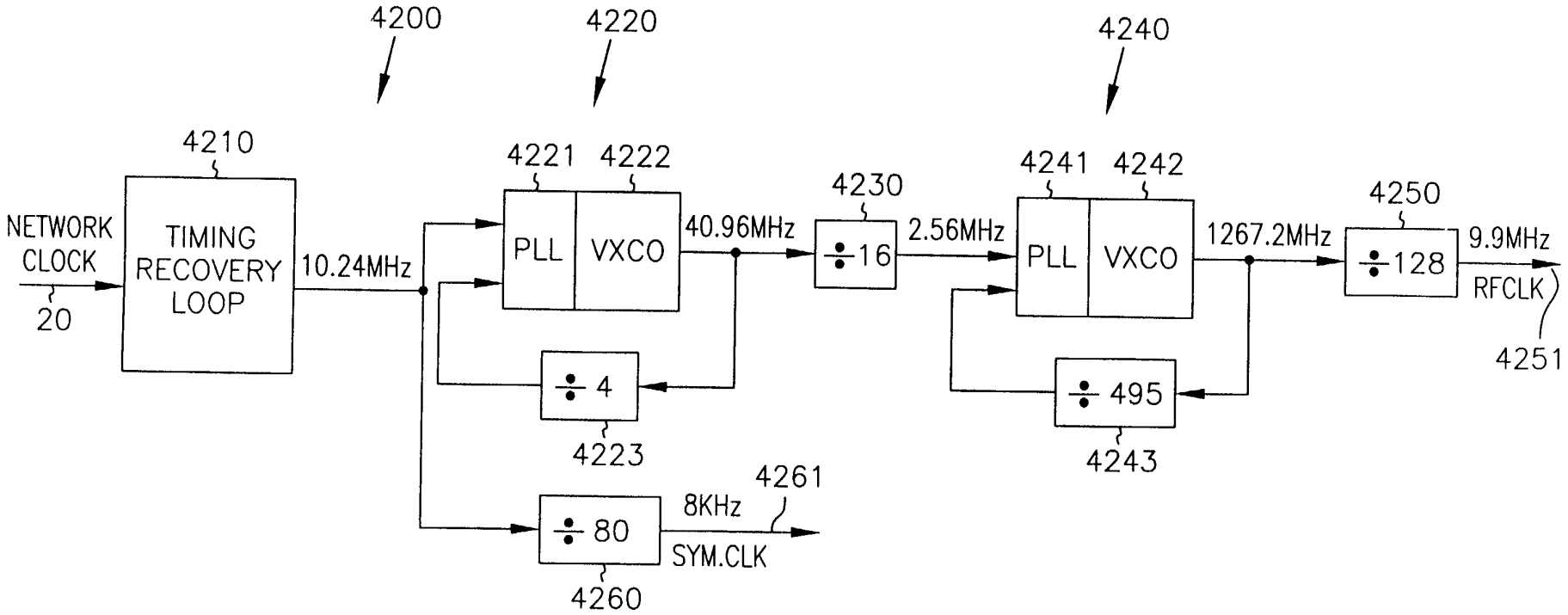


FIG. 51

Patent Application Publication

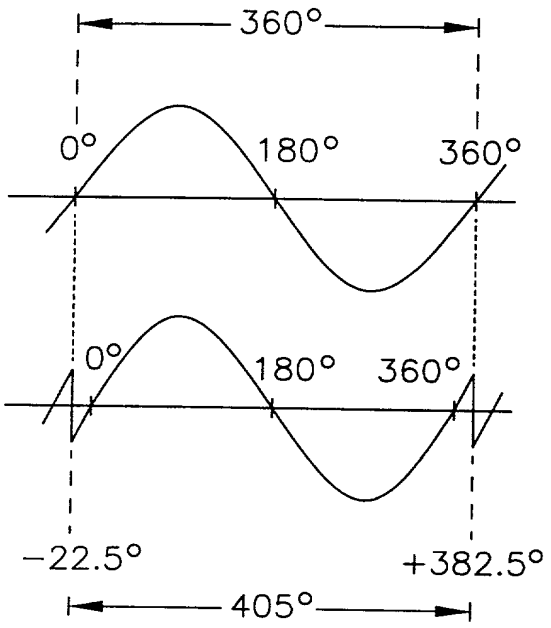


FIG. 52

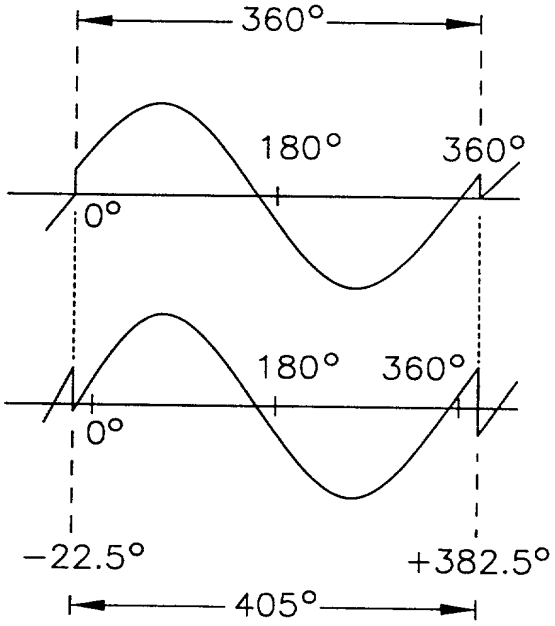


FIG. 53

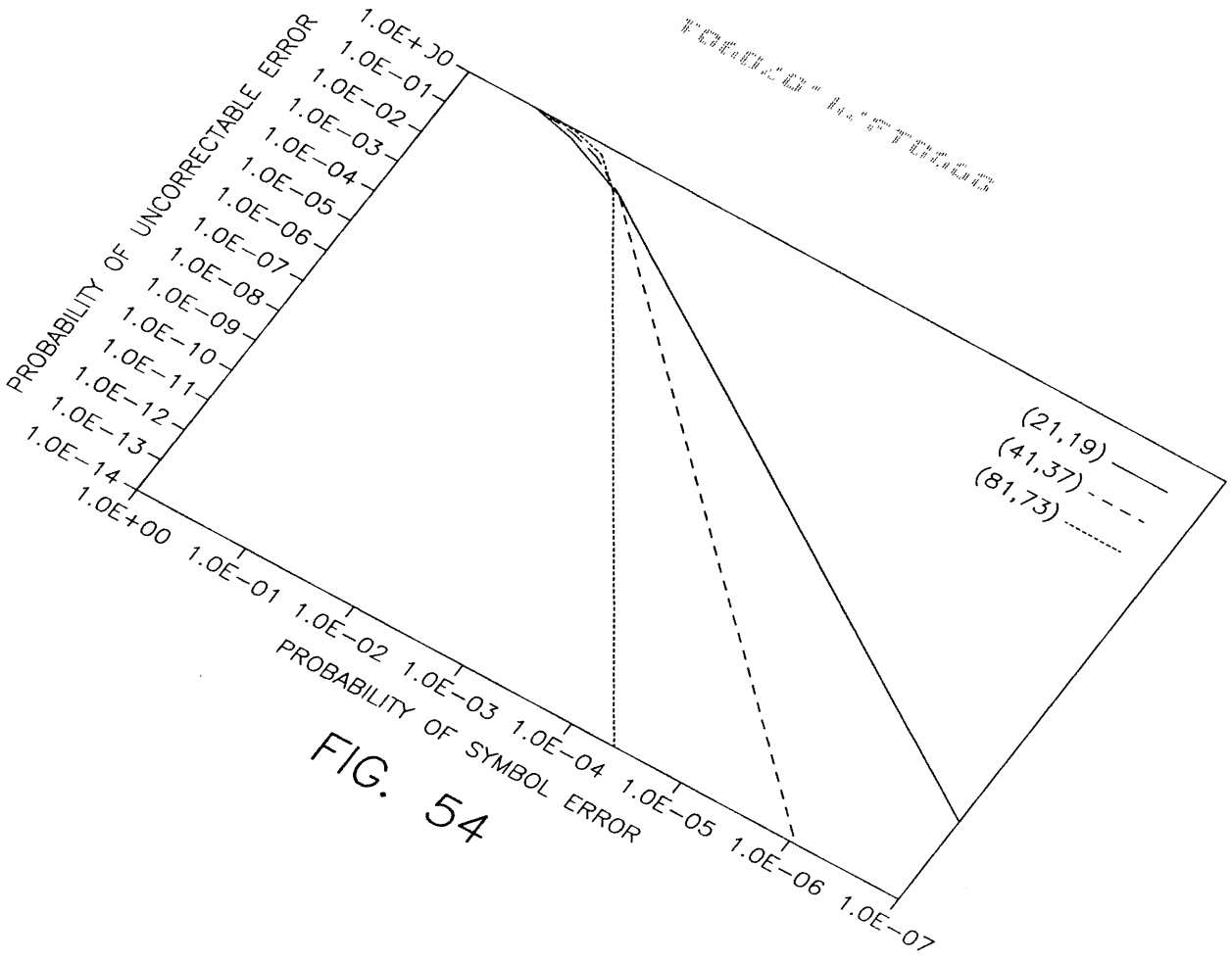

PROBABILITY OF UNCORRECTABLE ERROR
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
1.0E-13
1.0E-14
1.0E+00 1.0E-01 1.0E-02 1.0E-03 1.0E-04 1.0E-05 1.0E-06 1.0E-07
PROBABILITY OF SYMBOL ERROR
(21,19)
(41,37)
(81,73)

FIG. 54

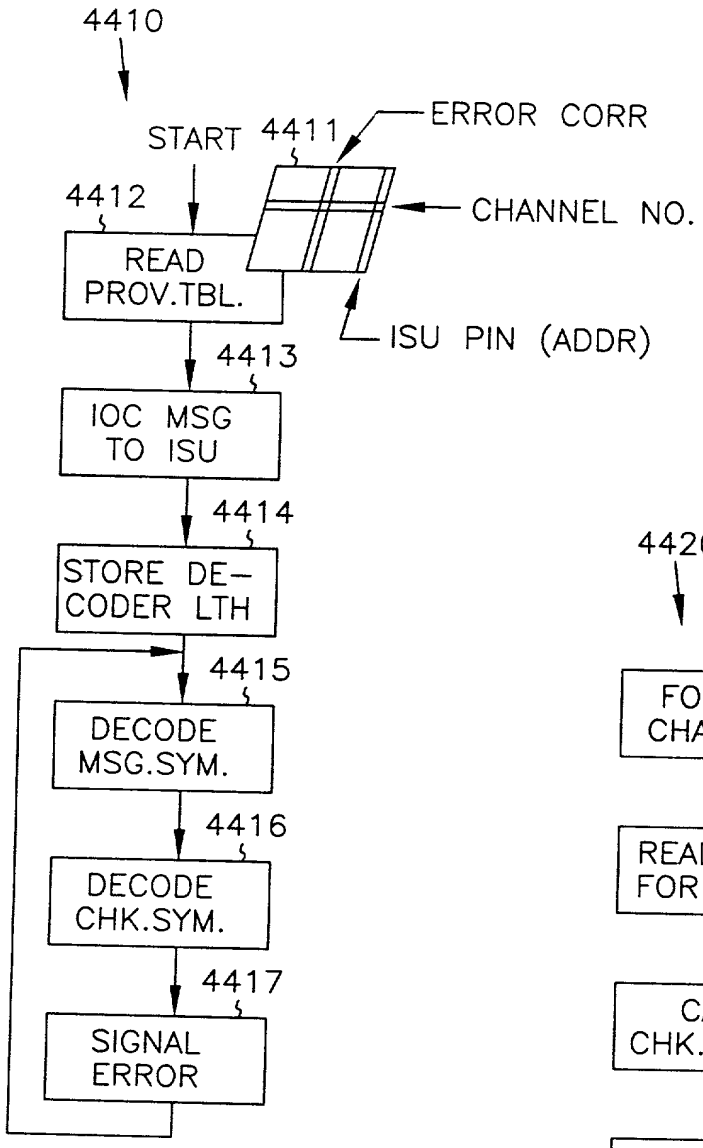


FIG. 55

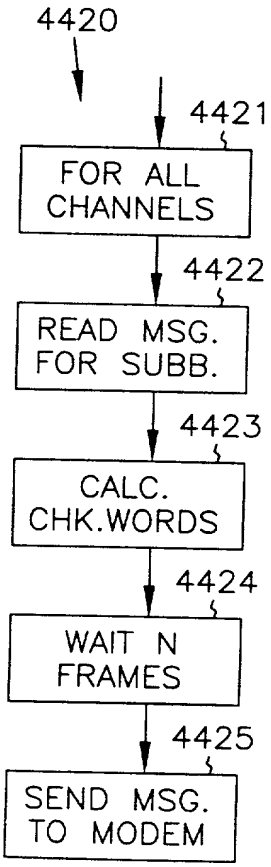


FIG. 56

Patent Application Publication

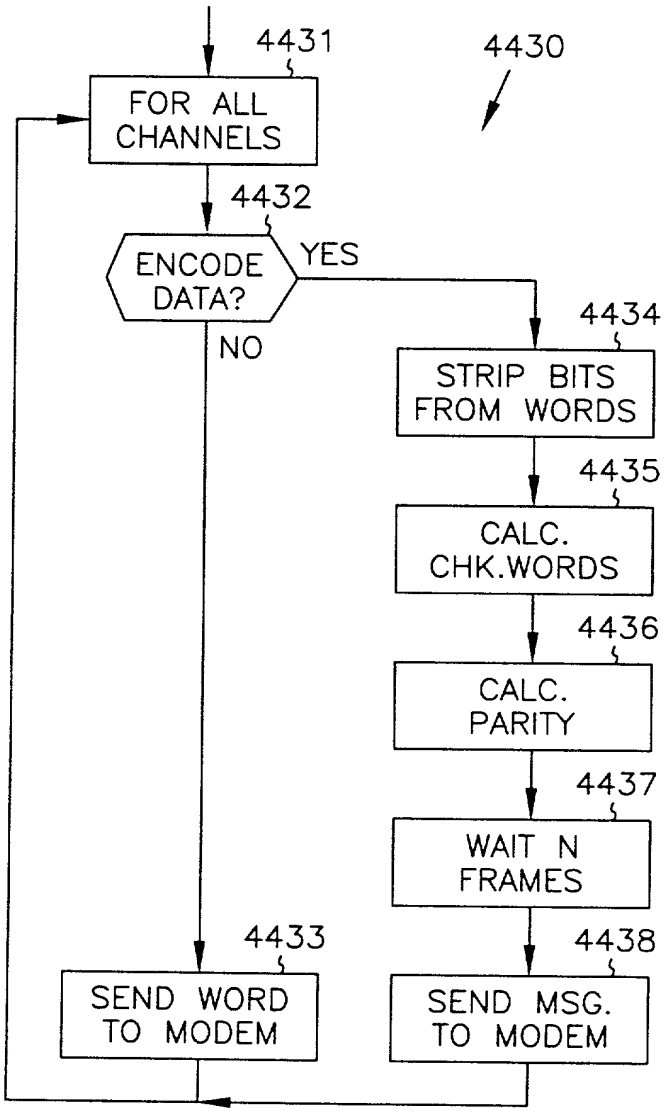

4431
4430
FOR ALL CHANNELS
4432
ENCODE DATA?
YES
NO
4434
STRIP BITS FROM WORDS
4435
CALC. CHK.WORDS
4436
CALC. PARITY
4437
WAIT N FRAMES
4433
4438
SEND WORD TO MODEM
SEND MSG. TO MODEM

FIG. 57

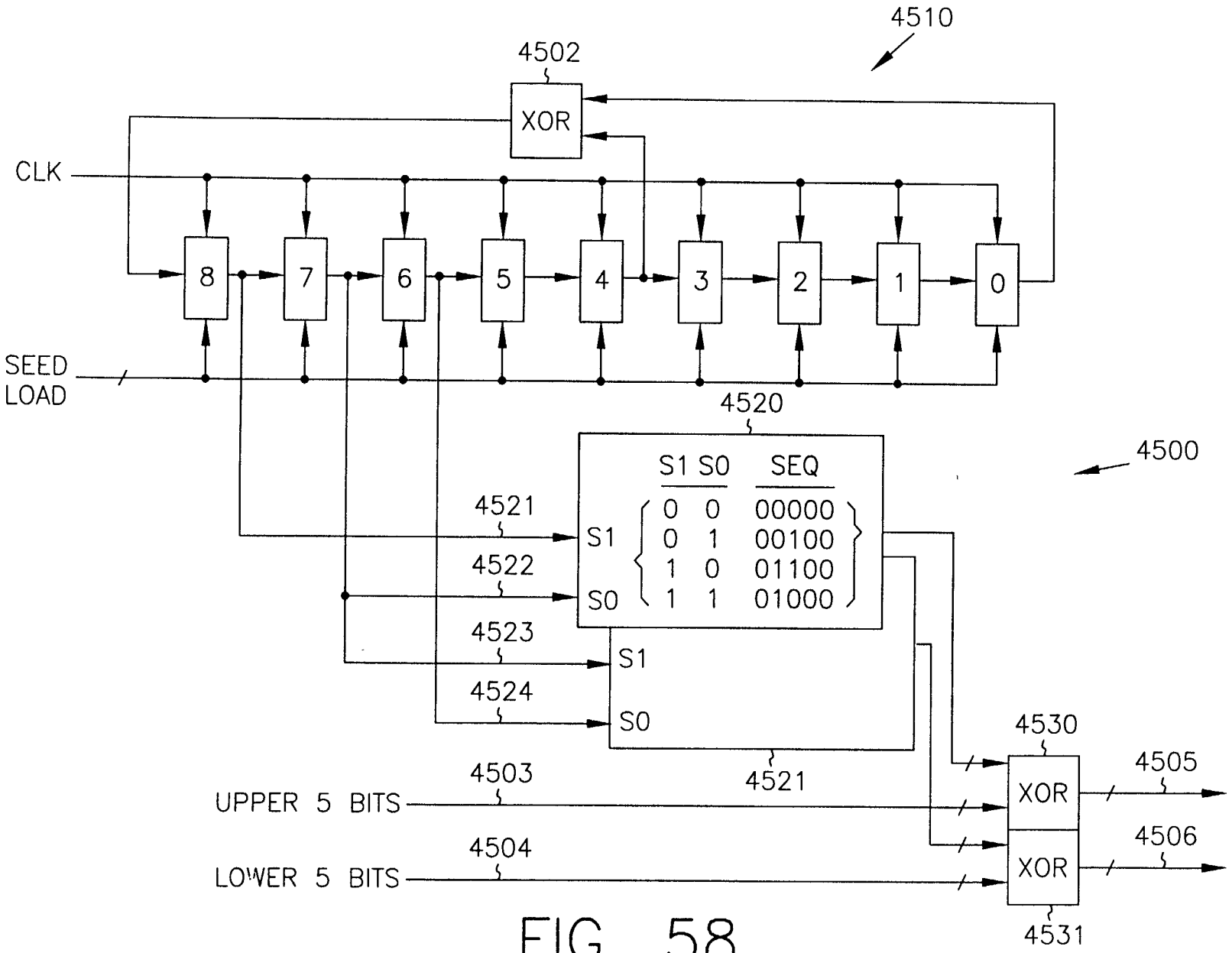

4510
4502
XOR
CLK
8
7
6
5
4
3
2
1
0
SEED
LOAD
4520
4500
S1 S0 SEQ
0 0 00000
0 1 00100
1 0 01100
1 1 01000
4521
S1
4522
S0
4523
S1
4524
S0
4521
4530
4503
UPPER 5 BITS
4504
LOWER 5 BITS
XOR
XOR
4505
4506
4531

FIG. 58

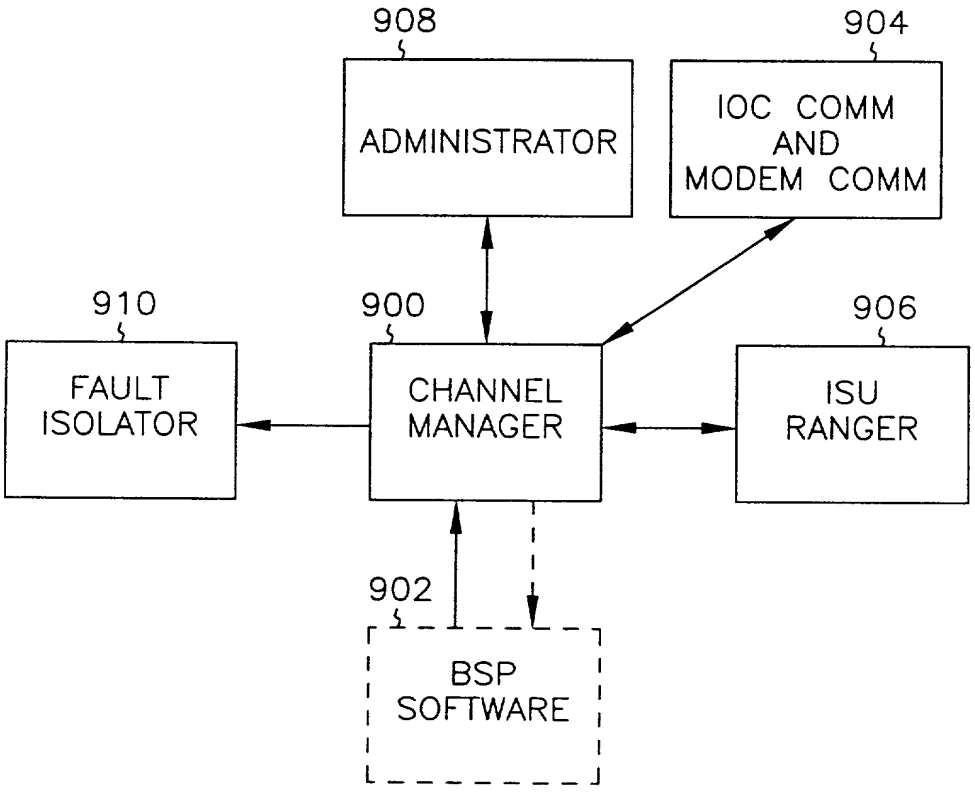

908
ADMINISTRATOR
904
IOC COMM
AND
MODEM COMM
910
FAULT
ISOLATOR
900
CHANNEL
MANAGER
906
ISU
RANGER
902
BSP
SOFTWARE

FIG. 59

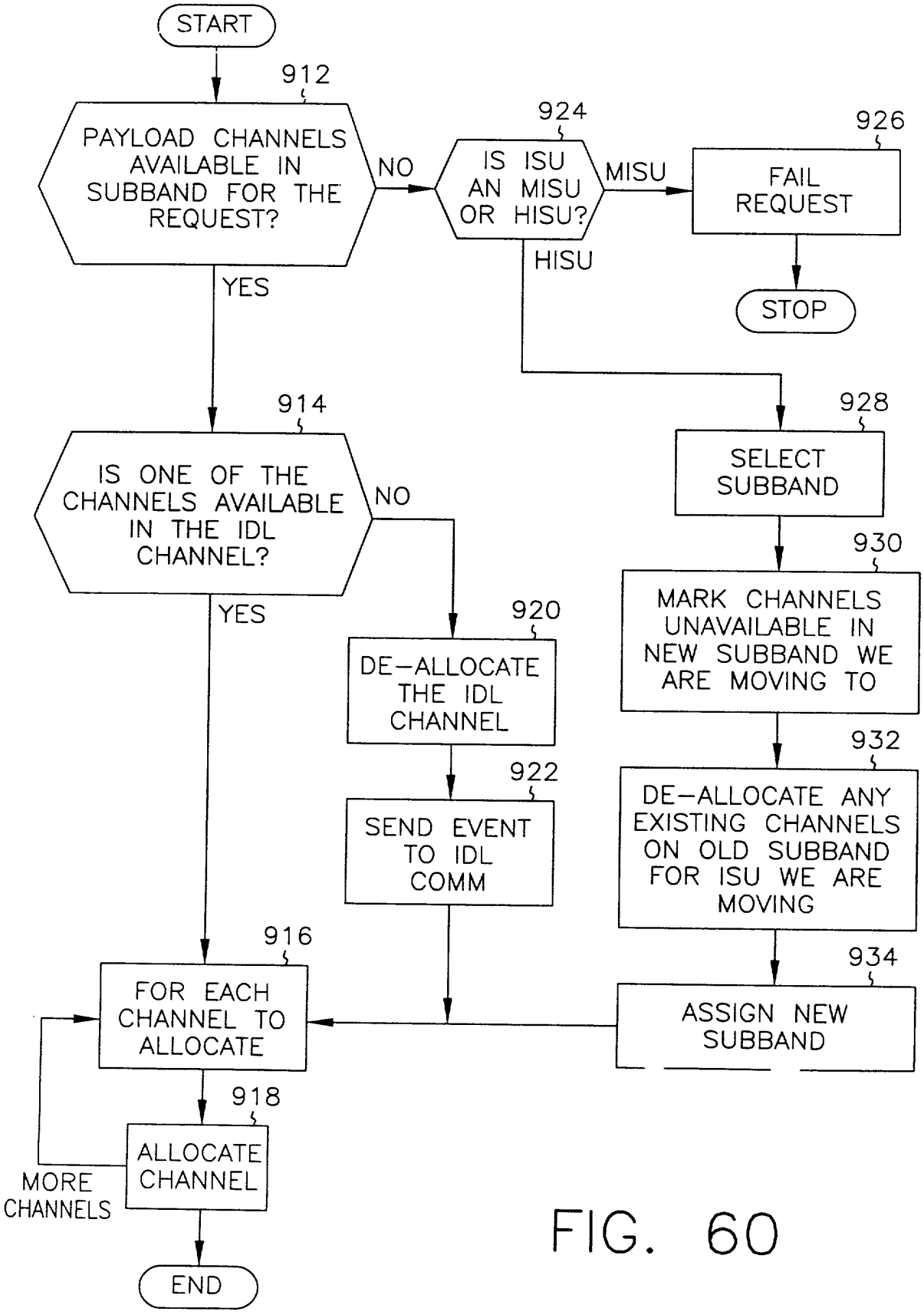

START
912
PAYLOAD CHANNELS AVAILABLE IN SUBBAND FOR THE REQUEST?
NO
924
IS ISU AN MISU OR HISU?
MISU
926
FAIL REQUEST
STOP
HISU
YES
914
IS ONE OF THE CHANNELS AVAILABLE IN THE IDL CHANNEL?
NO
928
SELECT SUBBAND
930
MARK CHANNELS UNAVAILABLE IN NEW SUBBAND WE ARE MOVING TO
YES
920
DE-ALLOCATE THE IDL CHANNEL
922
SEND EVENT TO IDL COMM
932
DE-ALLOCATE ANY EXISTING CHANNELS ON OLD SUBBAND FOR ISU WE ARE MOVING
916
FOR EACH CHANNEL TO ALLOCATE
934
ASSIGN NEW SUBBAND
918
ALLOCATE CHANNEL
MORE CHANNELS
END

FIG. 60

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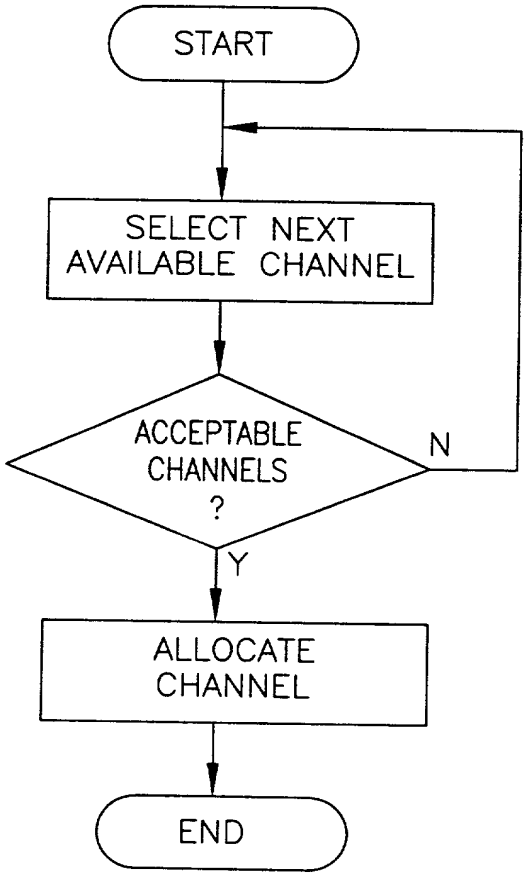


FIG. 61

EXPRESS MAIL NO. EV339126543US

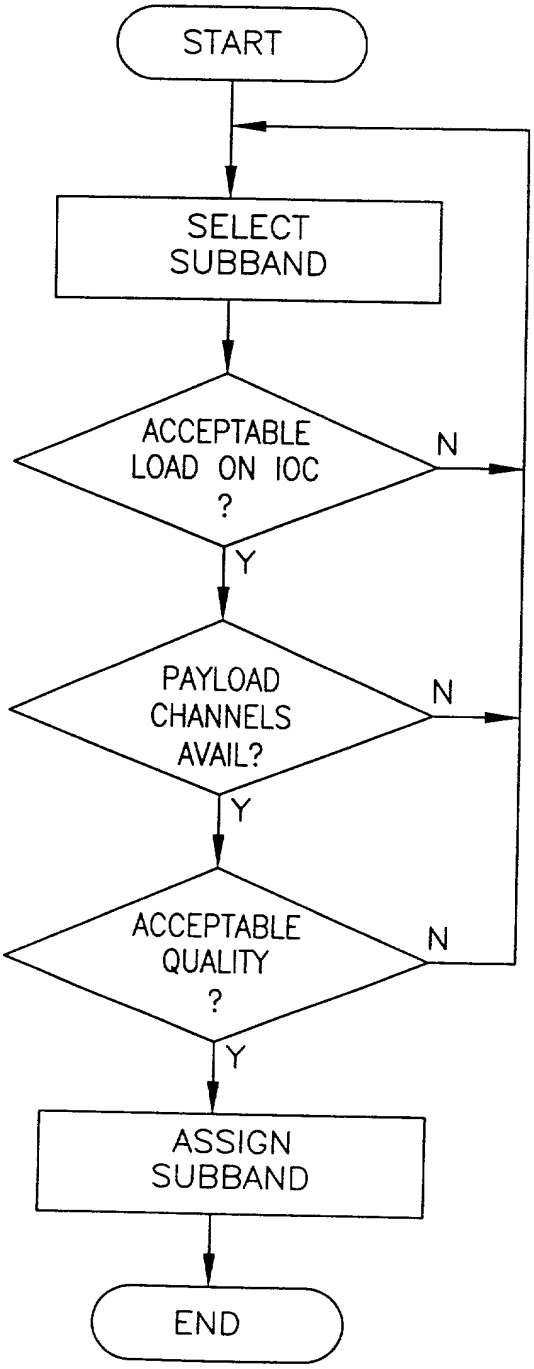


FIG. 62

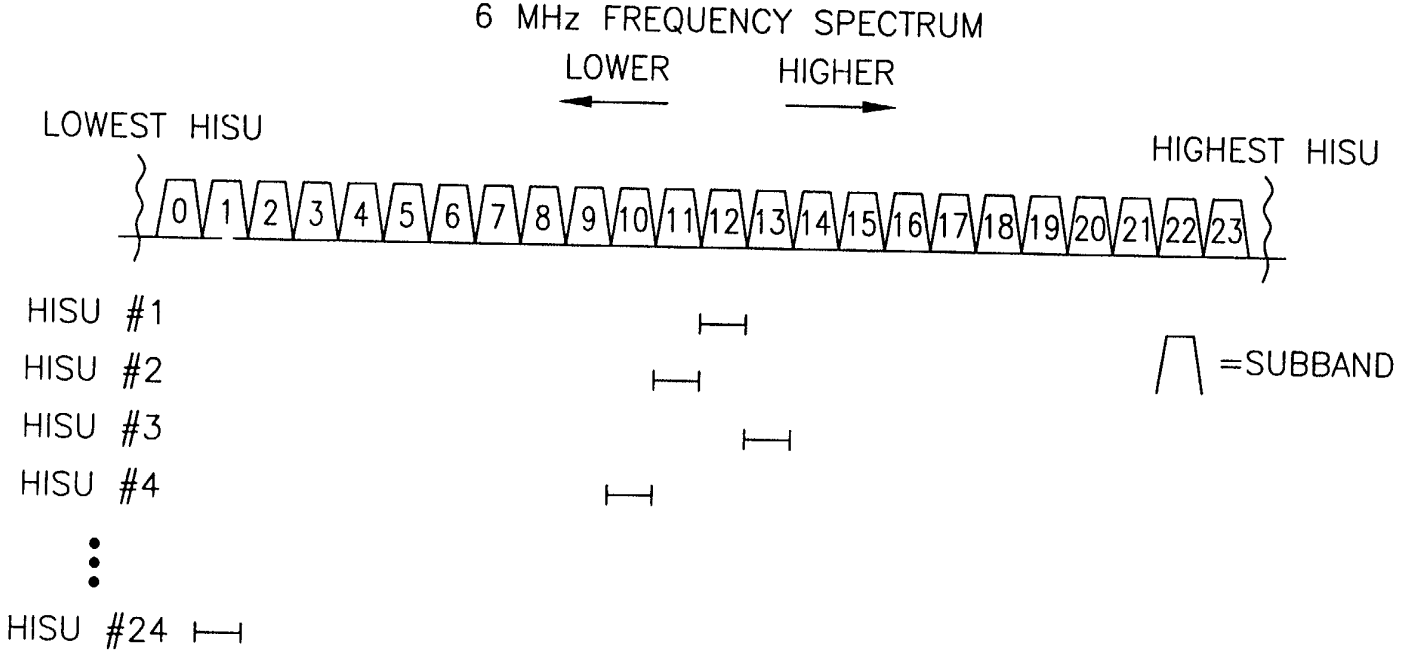

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
LOWEST HISU
HIGHEST HISU
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
HISU #1
HISU #2
HISU #3
HISU #4
HISU #24
=SUBBAND

FIG. 63

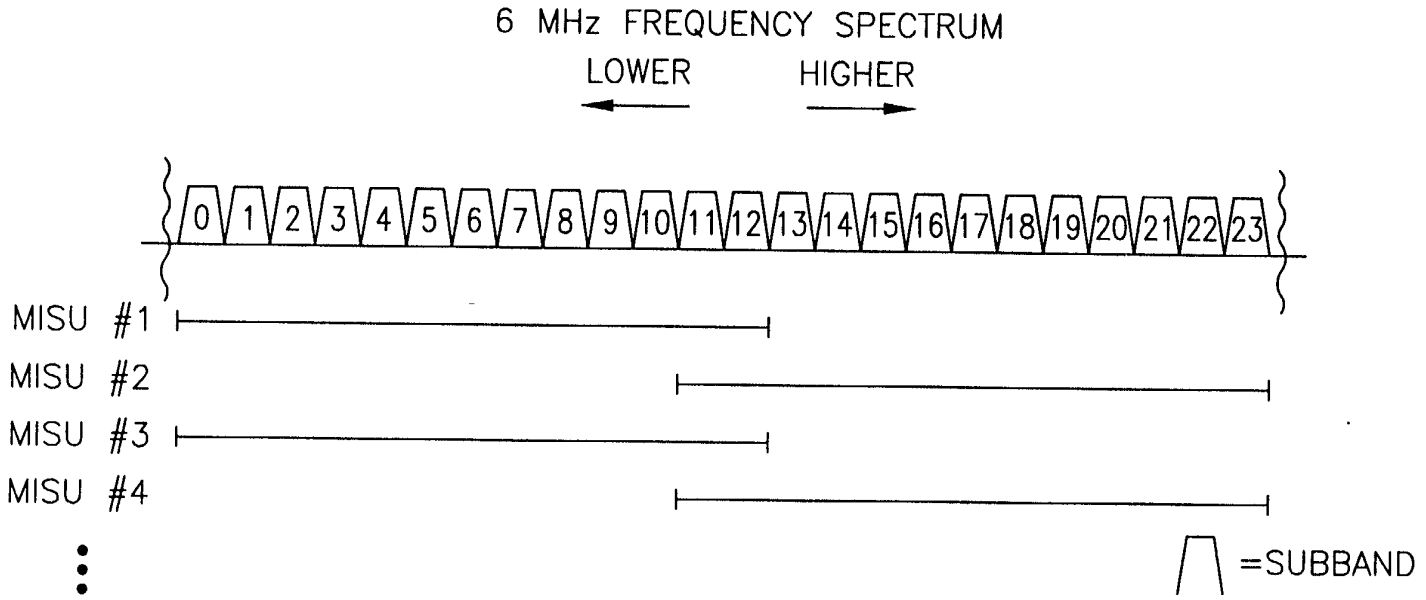

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
MISU #1
MISU #2
MISU #3
MISU #4
=SUBBAND

FIG. 64

T0620 "h2ST0669

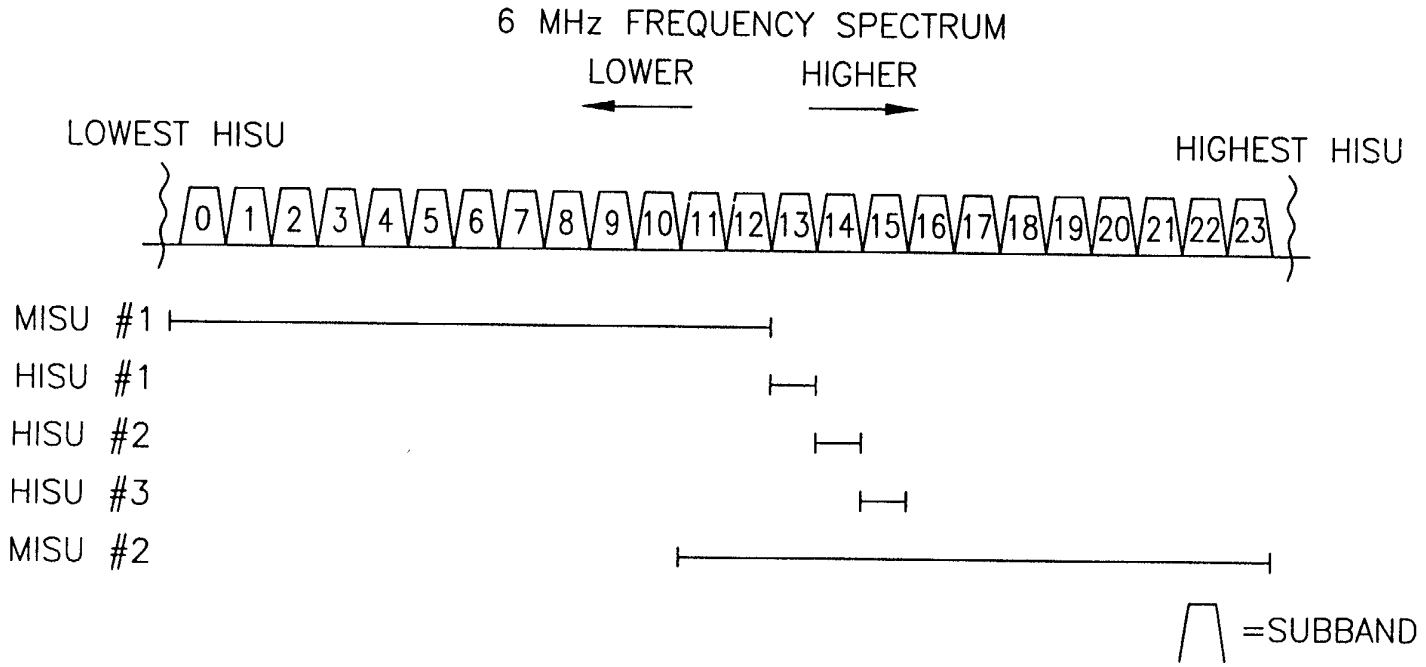


FIG. 65

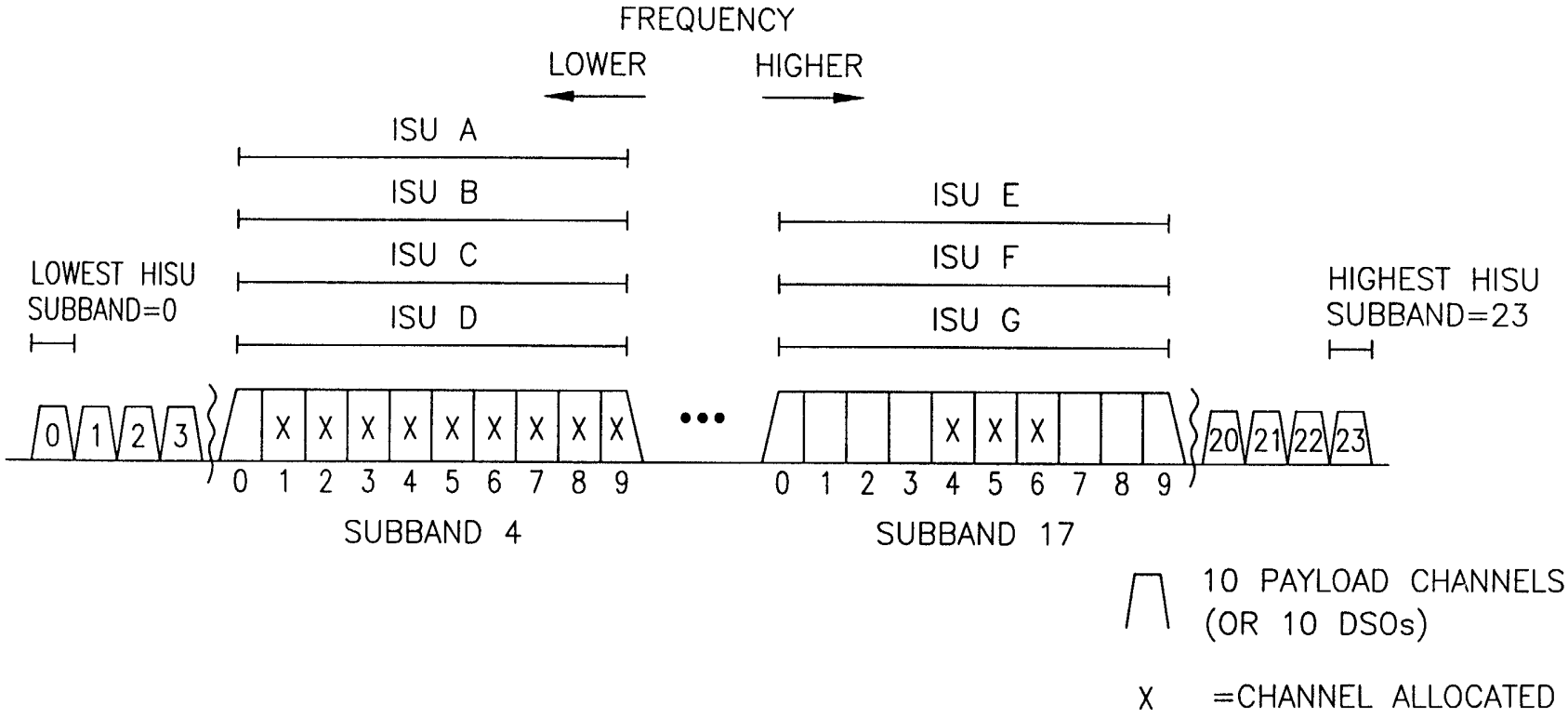

FREQUENCY
LOWER
HIGHER
ISU A
ISU B
ISU C
ISU D
ISU E
ISU F
ISU G
LOWEST HISU
SUBBAND=0
HIGHEST HISU
SUBBAND=23
0 1 2 3
X X X X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 4
X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 17
20 21 22 23
10 PAYLOAD CHANNELS
(OR 10 DSOs)
X =CHANNEL ALLOCATED

FIG. 66

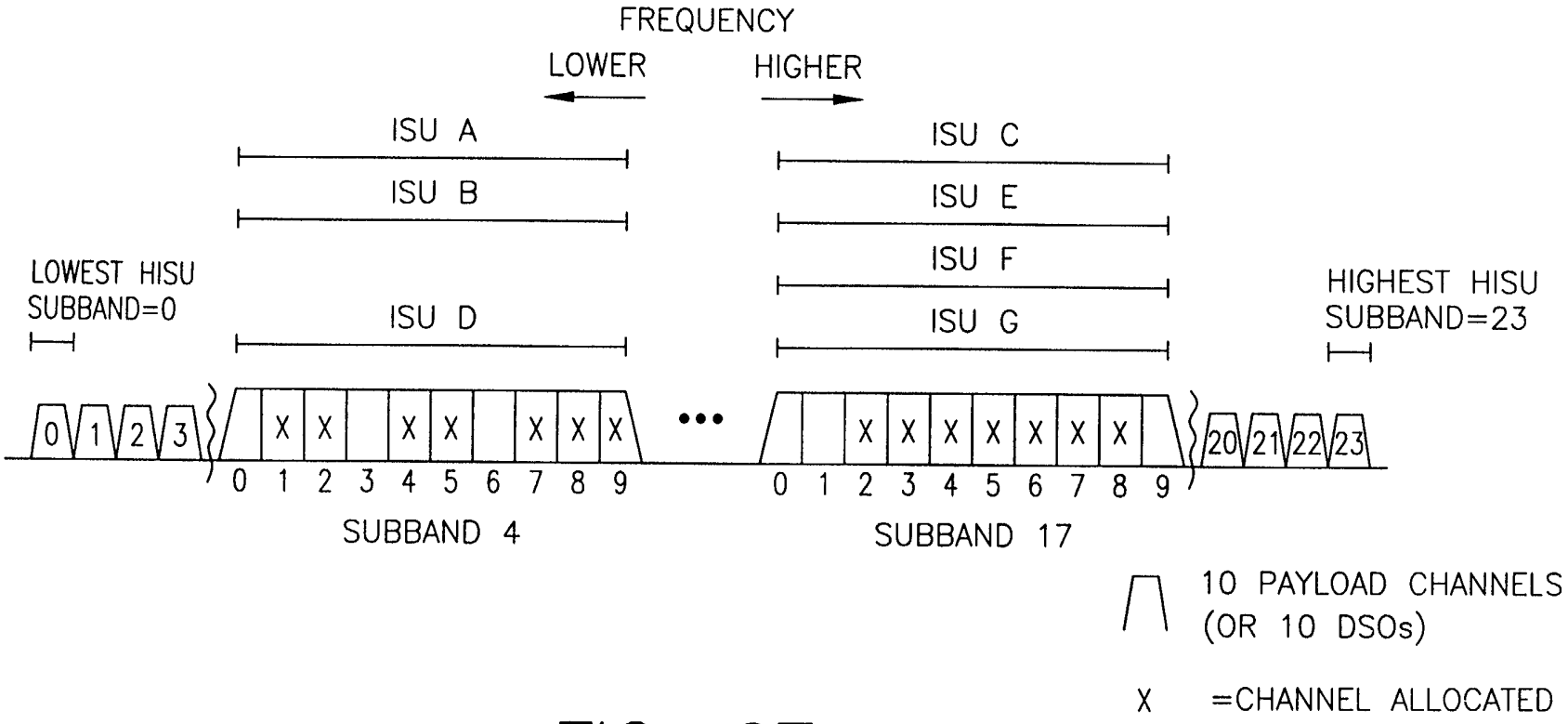

FREQUENCY
LOWER
HIGHER
ISU A
ISU B
ISU C
ISU E
ISU F
ISU D
ISU G
LOWEST HISU
SUBBAND=0
HIGHEST HISU
SUBBAND=23
0 1 2 3
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 4
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 17
20 21 22 23
10 PAYLOAD CHANNELS
(OR 10 DSOs)
X =CHANNEL ALLOCATED

FIG. 67

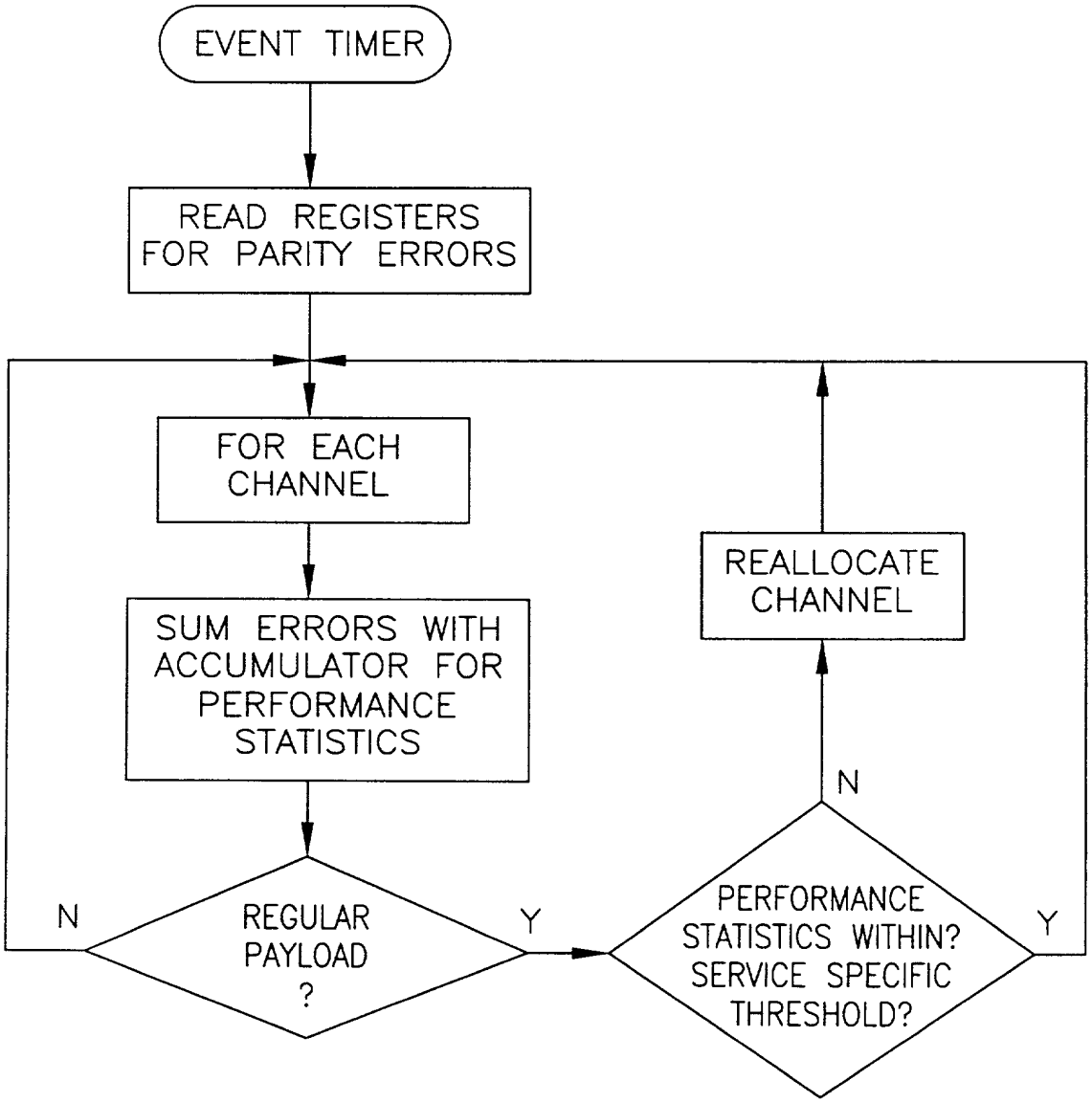

EVENT TIMER
READ REGISTERS FOR PARITY ERRORS
FOR EACH CHANNEL
SUM ERRORS WITH ACCUMULATOR FOR PERFORMANCE STATISTICS
REGULAR PAYLOAD ?
N
Y
PERFORMANCE STATISTICS WITHIN? SERVICE SPECIFIC THRESHOLD?
N
Y
REALLOCATE CHANNEL

FIG. 68

PACSYS-1425-0050

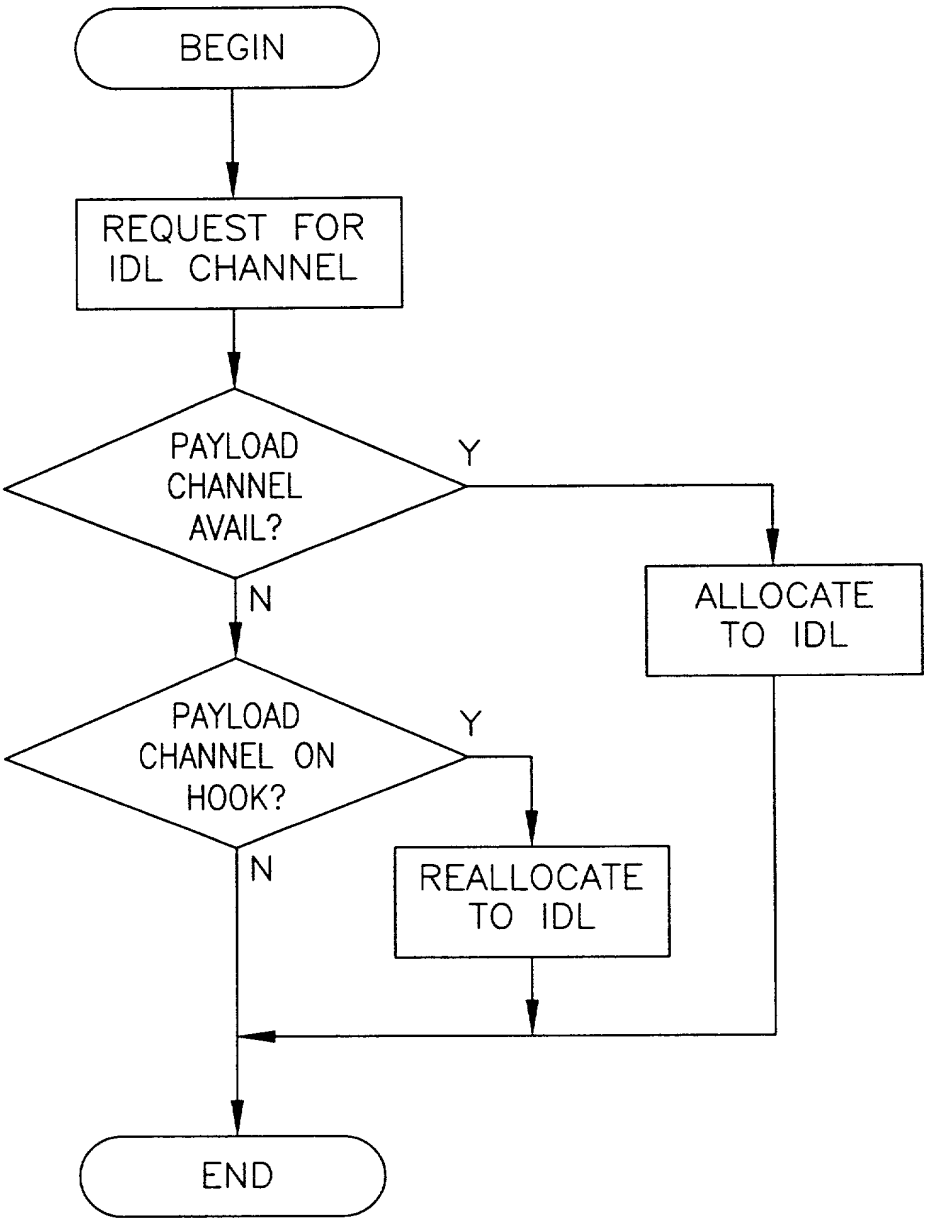


FIG. 69

T06020"h2ST0660

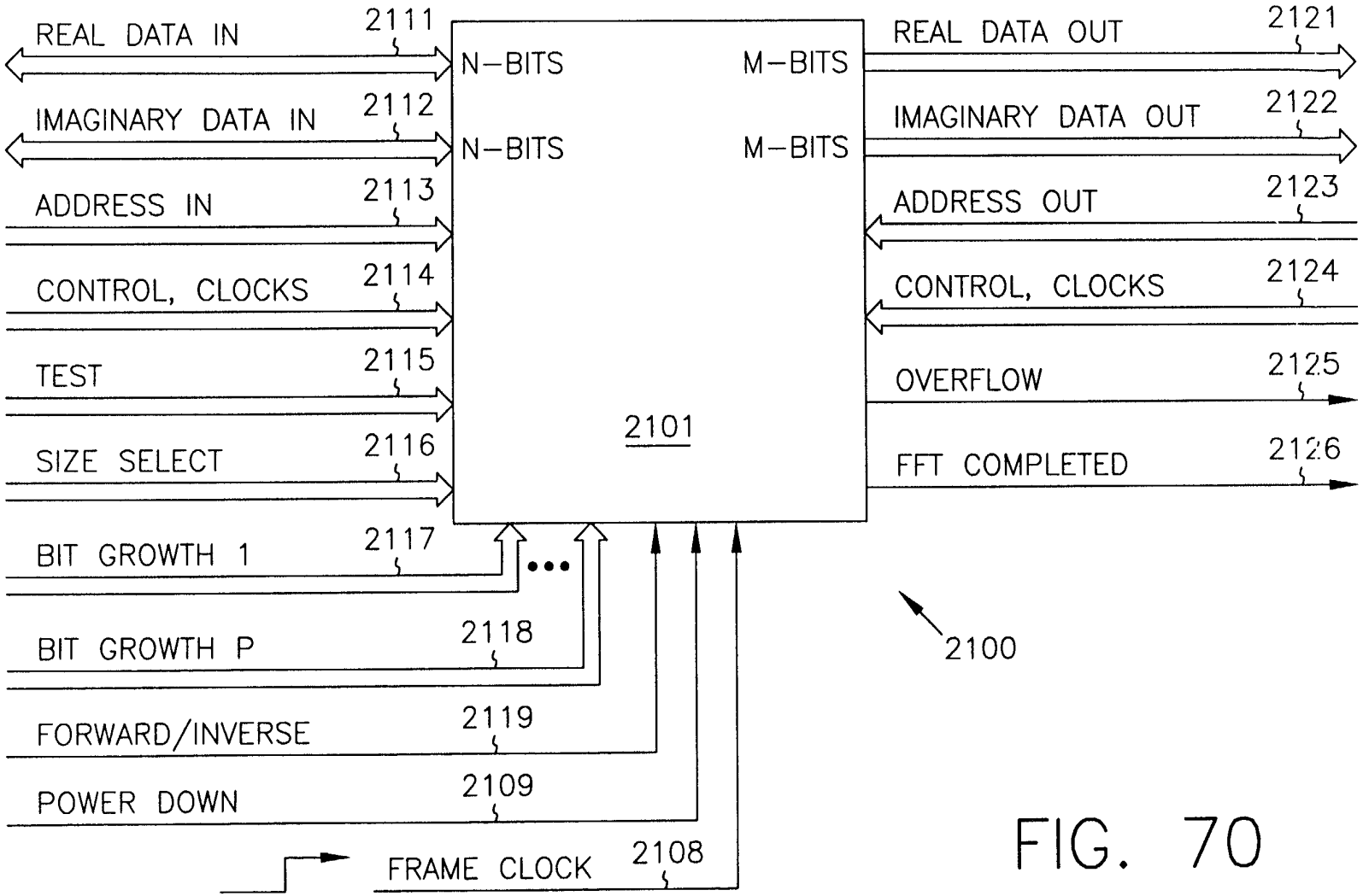


FIG. 70

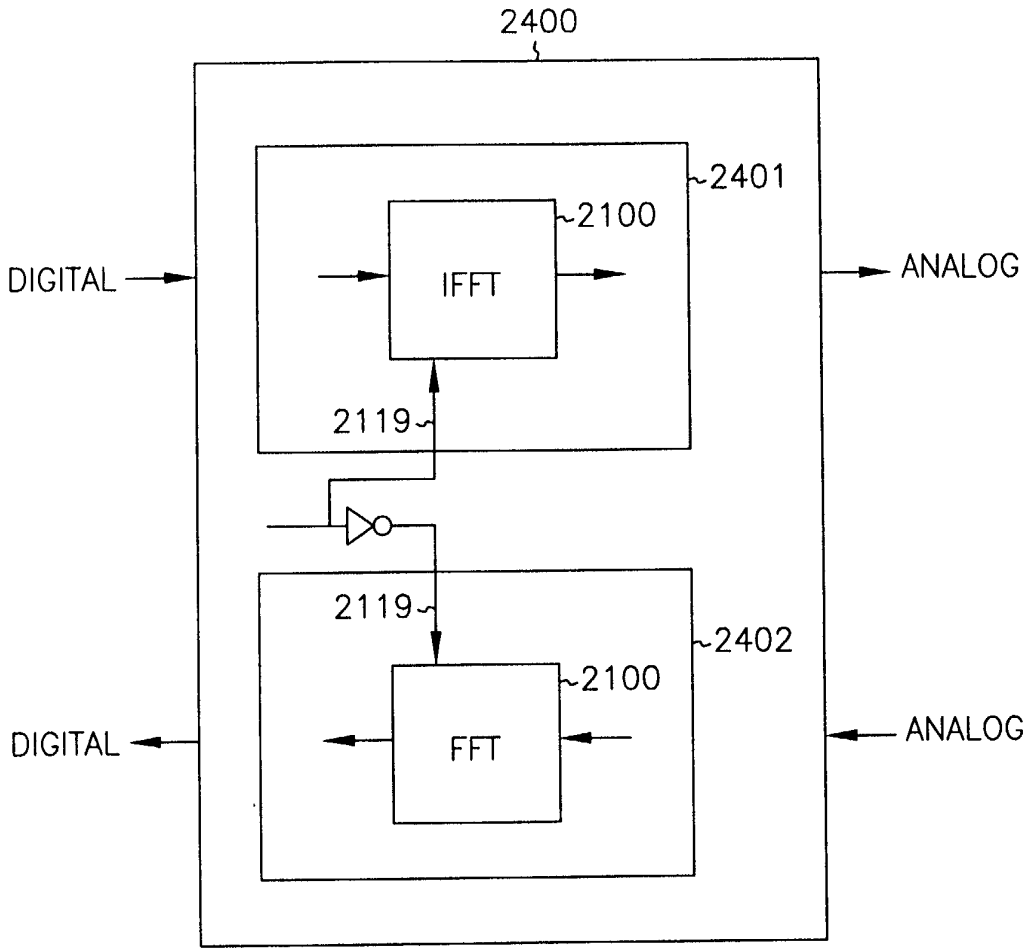

2400
2401
2100
IFFT
DIGITAL
ANALOG
2119
2119
2402
2100
FFT
DIGITAL
ANALOG

FIG. 71

T06020"h2ET0660

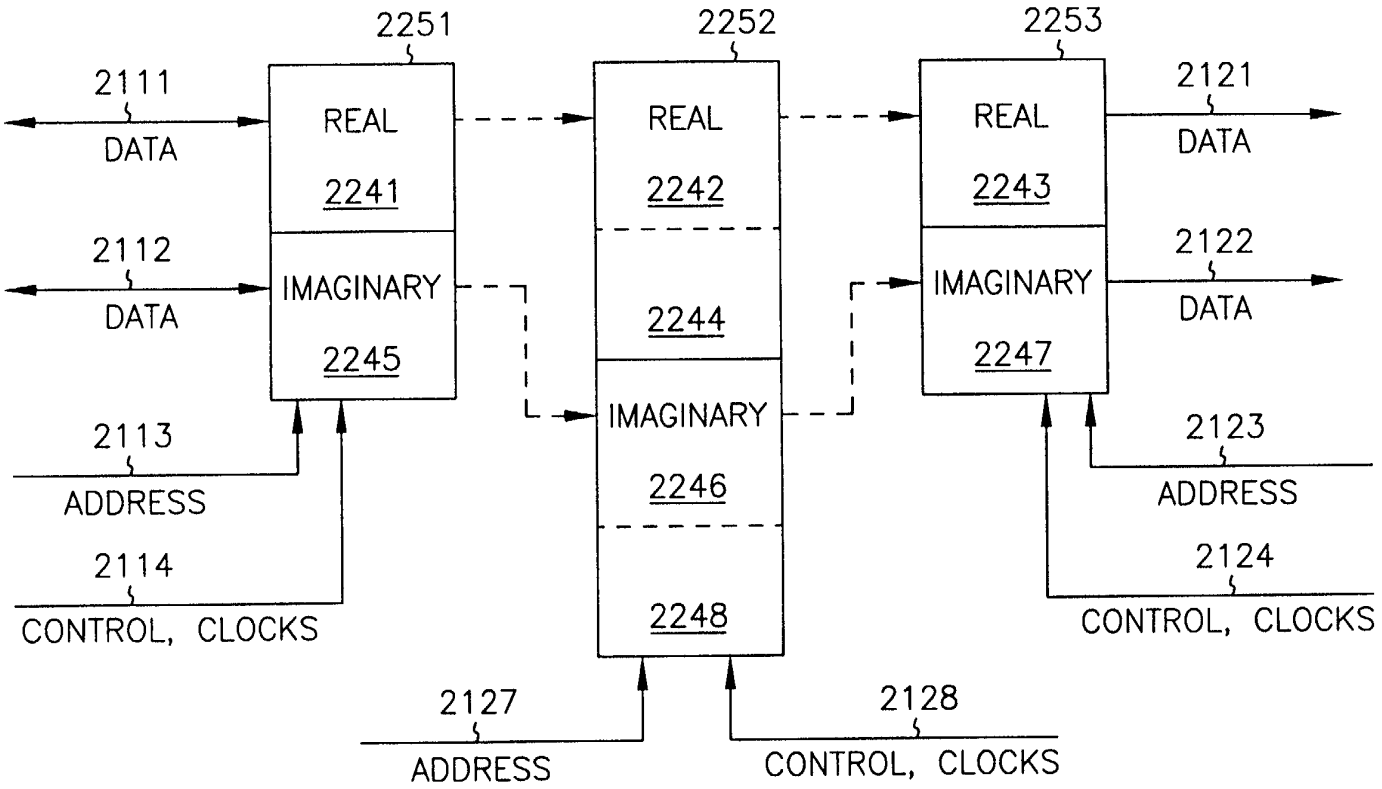


FIG. 72

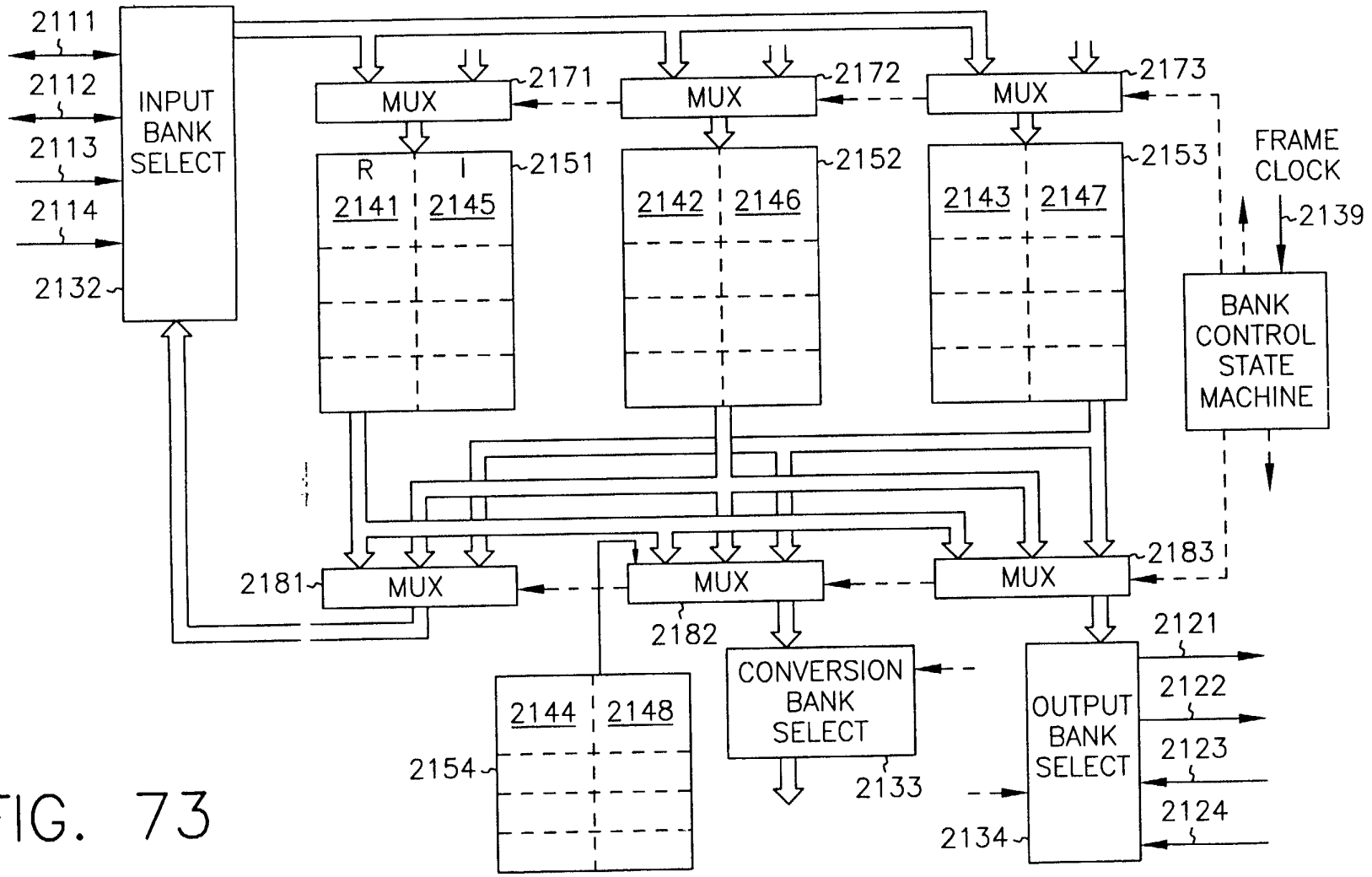
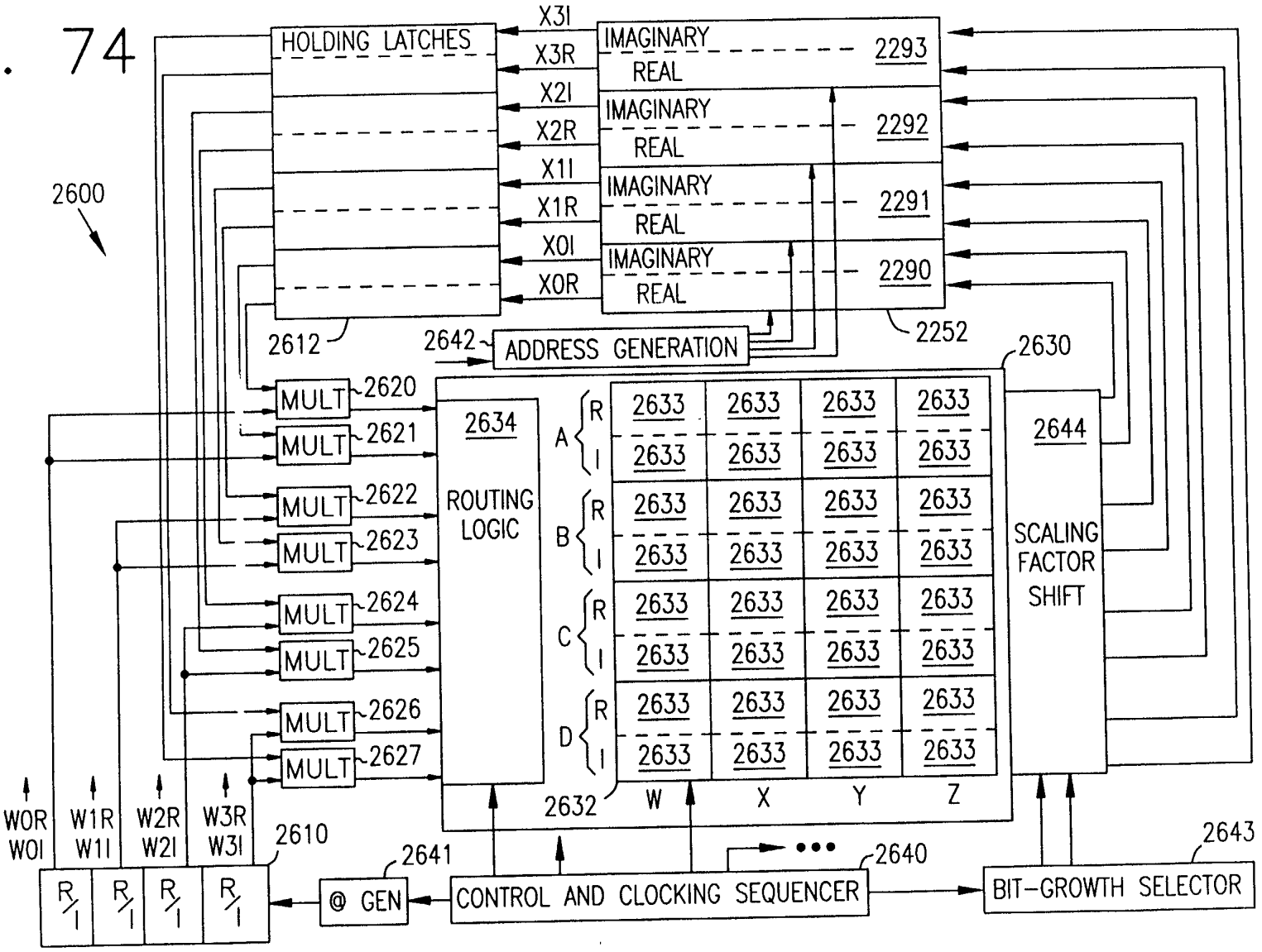

2111
2112
2113
2114
2132
INPUT BANK SELECT
MUX
2171
MUX
2172
MUX
2173
FRAME CLOCK
2139
R
I
2141
2145
2151
2142
2146
2152
2143
2147
2153
BANK CONTROL STATE MACHINE
2181
MUX
MUX
MUX
2183
2182
2121
2122
2123
2124
CONVERSION BANK SELECT
2133
OUTPUT BANK SELECT
2134
2144
2148
2154

FIG. 73

FIG. 74


2600
HOLDING LATCHES
X3I
X3R
X2I
X2R
X1I
X1R
X0I
X0R
IMAGINARY
REAL
2293
2292
2291
2290
2252
2612
2642
ADDRESS GENERATION
2630
MULT
2620
2621
2622
2623
2624
2625
2626
2627
2634
ROUTING LOGIC
A
B
C
D
R
I
2633
W
X
Y
Z
2632
2644
SCALING FACTOR SHIFT
W0R
W0I
W1R
W1I
W2R
W2I
W3R
W3I
2610
R/I
@ GEN
2641
CONTROL AND CLOCKING SEQUENCER
2640
BIT-GROWTH SELECTOR
2643

THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

CO

AWR=WR AWI =WI	AXR=XR AXI =XI	AYR=YR AYI =YI	AZR=ZR AZI =ZI
BWR=WR BWI =WI	BXR=XR BXI =XI	BYR=YR BYI =YI	BZR=ZR BZI =ZI
CWR=WR CWI =WI	CXR=XR CXI =XI	CYR=YR CYI =YI	CZR=ZR CZI =ZI
DWR=WR DWI =WI	DXR=XR DXI =XI	DYR=YR DYI =YI	DZR=ZR DZI =ZI

2632

2800

FIG. 75

CI

AWR=AWR −WI AWI=AWI +WR	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR −ZI DZI=DZI +ZR

2632

2800

FIG. 76

C2

AWR=AWR +WR AWI=AWI +WI	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR −ZI DZI=DZI +ZR

2632

2800

FIG. 77

C3

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XR AXI=AXI +XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XR BXI=BXI +XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XR CXI=CXI +XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XR DXI=DXI +XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI −ZI

2632

2800

FIG. 78

C4

AWR=AWR +WR AWI=AWI +WI	AXR=AXR --XR AXI=AXI −XI	AYR=AYR +YR AYI=AYI +YI	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YR BYI=BYI +YI	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YR CYI=CYI +YI	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YR DYI=DYI +YI	DZR=DZR −ZR DZI=DZI −ZI

2632

2800

FIG. 79

C5

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR +ZI DZI=DZI −ZR

2632

2800

FIG. 80

C6

AWR=AWR +WR AWI=AWI +WI	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR +ZI DZI=DZI −ZR

2632

2800

FIG. 81

C7

AWR=AWR −WI AWI=AWI +WR	AXR=AXR −XR AXI=AXI −XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI +ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI +ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI +ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI +ZI

2632

2800

FIG. 82

THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

C0

2632

AWR =WR+XR+YR+ZR AWI =WI+XI+YI+ZI	AXR =WR−XI−YR+ZI AXI =WI+XR−YI−ZR	AYR =WR−XR+YR−ZR AYI =WI−XI+YI−ZI	AZR =WR+XI−YR−ZI AZI =WI−XR−YI+ZR
− −	− −	− −	− −
− −	− −	− −	− −
− −	− −	− −	− −

2810

FIG. 83

C1

2632

AWR =AWR−(WI+XI+YI+ZI) AWI =AWI+(WR+XR+YR+ZR)	AXR =AXR−(WI+XR−YI−ZR) AXI =AXI+(WR−XI−YR+ZI)	AYR =AYR−(WI−XI+YI−ZI) AYI =AYI+(WR−XR+YR−ZR)	AZR =AZR−(WI−XR−YI+ZR) AZI =AZI+(WR+XI−YR−ZI)
− −	− −	− −	− −
− −	− −	− −	− −
− −	− −	− −	− −

2810

FIG. 84

C2

2632

2810

– –	– –	– –	– –
BWR =WR+XR+YR+ZR BWI =WI+XI+YI+ZI	BXR =WR−XI−YR+ZI BXI =WI+XR−YI−ZR	BYR =WR−XR+YR−ZR BYI =WI−XI+YI−ZI	BZR =WR+XI−YR−ZI BZI =WI−XR−YI+ZR
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 85

C3

2632

2810

– –	– –	– –	– –
BWR =BWR−(WI+XI+YI+ZI) BWI =BWI+(WR+XR+YR+ZR)	BXR =BXR−(WI+XR−YI−ZR) BXI =BXI+(WR−XI−YR+ZI)	BYR =BYR−(WI−XI+YI−ZI) BYI =BYI+(WR−XR+YR−ZR)	BZR =BZR−(WI−XR−YI+ZR) BZI =BZI+(WR+XI−YR−ZI)
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 86

C4

2632

2810

– –	– –	– –	– –
– –	– –	– –	– –
CWR =WR+XR+YR+ZR CWI =WI+XI+YI+ZI	CXR =WR−XI−YR+ZI CXI =WI+XR−YI−ZR	CYR =WR−XR+YR−ZR CYI =WI−XI+YI−ZI	CZR =WR+XI−YR−ZI CZI =WI−XR−YI+ZR
– –	– –	– –	– –

FIG. 87

C5

2632

2810

– –	– –	– –	– –
– –	– –	– –	– –
CWR =CWR−(WI+XI+YI+ZI) CWI =CWI+(WR+XR+YR+ZR)	CXR =CXR−(WI+XR−YI−ZR) CXI =CXI+(WR−XI−YR+ZI)	CYR =CYR−(WI−XI+YI−ZI) CYI =CYI+(WR−XR+YR−ZR)	CZR =CZR−(WI−XR−YI+ZR) CZI =CZI+(WR+XI−YR−ZI)
– –	– –	– –	– –

FIG. 88

C6

2632

2810

–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
DWR =WR+XR+YR+ZR DWI =WI+XI+YI+ZI	DXR =WR−XI−YR+ZI DXI =WI+XR−YI−ZR	DYR =WR−XR+YR−ZR DYI =WI−XI+YI−ZI	DZR =WR+XI−YR−ZI DZI =WI−XR−YI+ZR

FIG. 89

C7

2632

2810

–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
DWR =DWR−(WI+XI+YI+ZI) DWI =DWI+(WR+XR+YR+ZR)	DXR =DXR−(WI+XR−YI−ZR) DXI =DXI+(WR−XI−YR+ZI)	DYR =DYR−(WI−XI+YI−ZI) DYI =DYI+(WR−XR+YR−ZR)	DZR =DZR−(WI−XR−YI+ZR) DZI =DZI+(WR+XI−YR−ZI)

FIG. 90

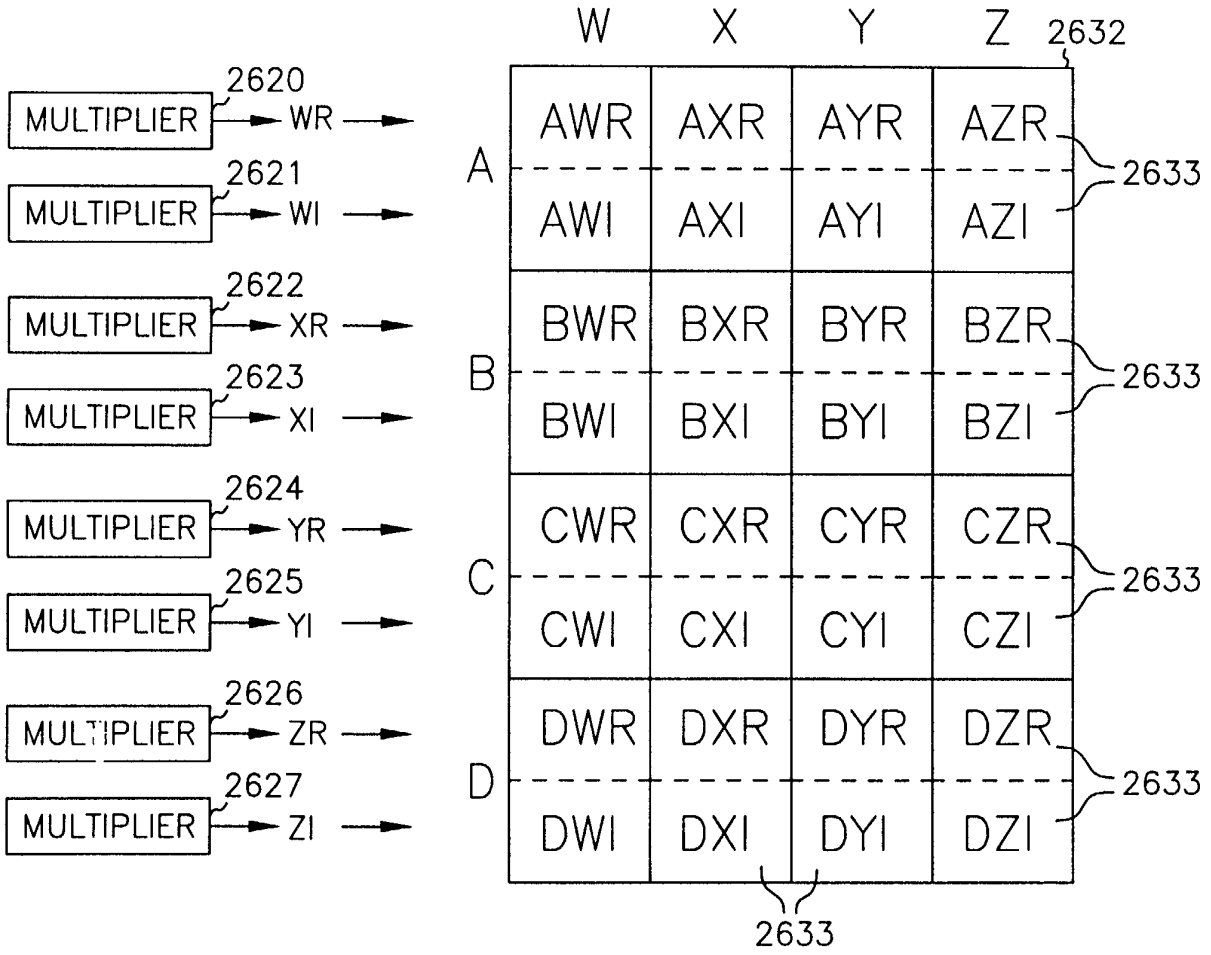

MULTIPLIER
2620
WR
MULTIPLIER
2621
WI
MULTIPLIER
2622
XR
MULTIPLIER
2623
XI
MULTIPLIER
2624
YR
MULTIPLIER
2625
YI
MULTIPLIER
2626
ZR
MULTIPLIER
2627
ZI
W
X
Y
Z
2632
A
B
C
D
AWR
AXR
AYR
AZR
AWI
AXI
AYI
AZI
BWR
BXR
BYR
BZR
BWI
BXI
BYI
BZI
CWR
CXR
CYR
CZR
CWI
CXI
CYI
CZI
DWR
DXR
DYR
DZR
DWI
DXI
DYI
DZI
2633
2633
2633
2633
2633

FIG. 91

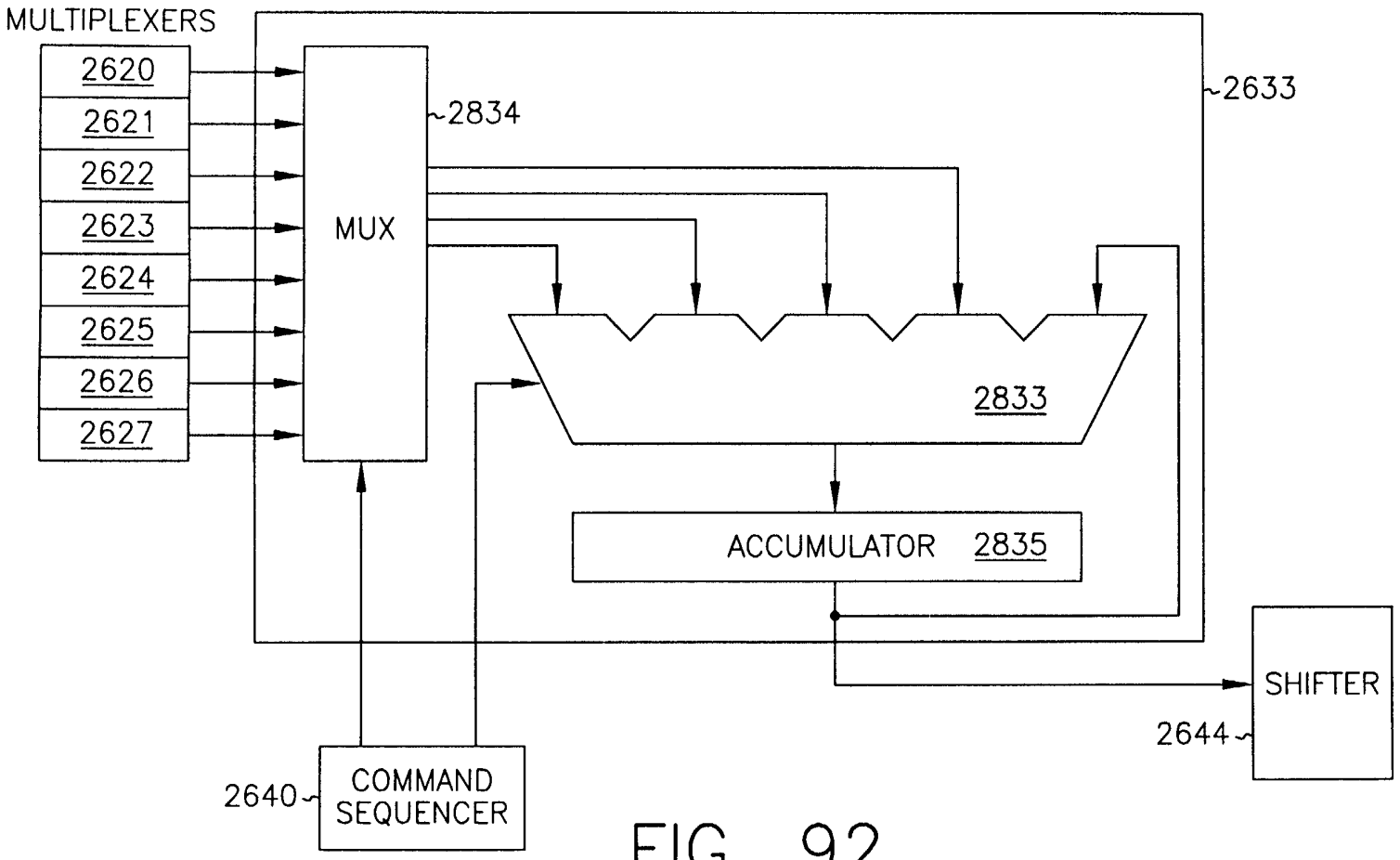

MULTIPLEXERS
2620
2621
2622
2623
2624
2625
2626
2627
MUX
2834
2633
2833
ACCUMULATOR 2835
SHIFTER
2644
2640
COMMAND SEQUENCER

FIG. 92

T0620"h2E0660

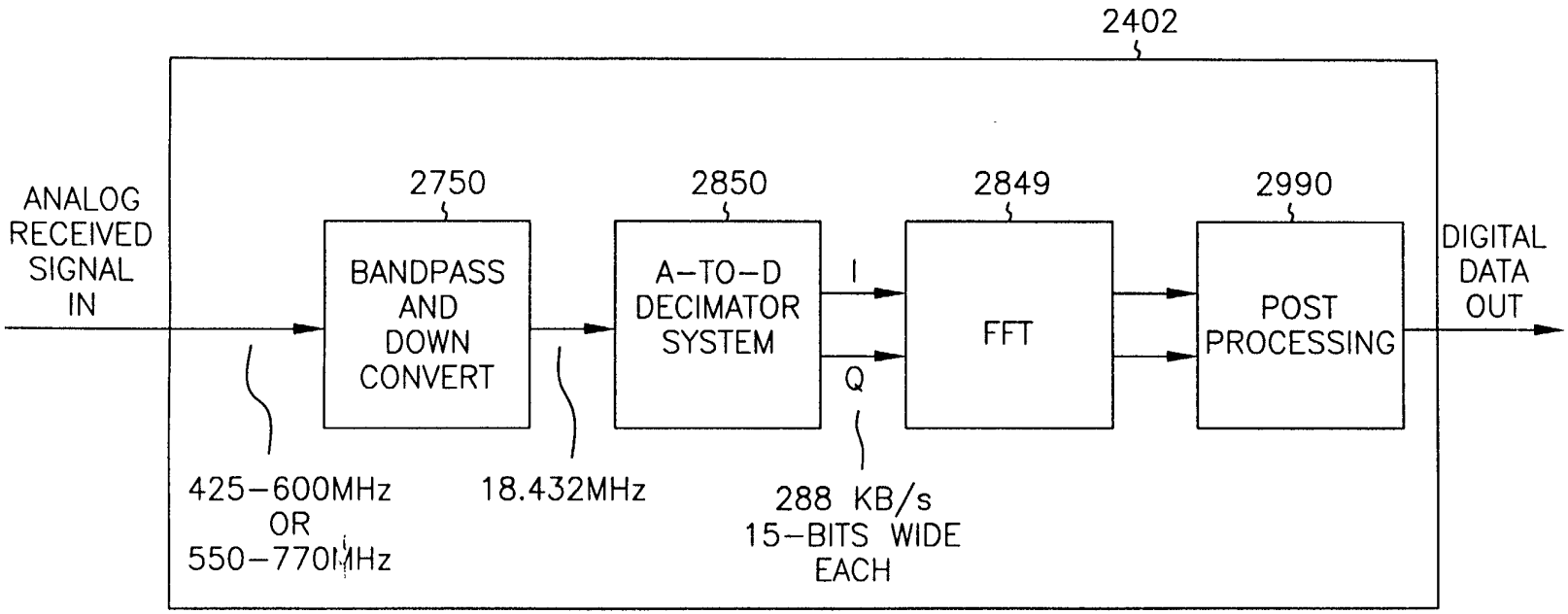


FIG. 93

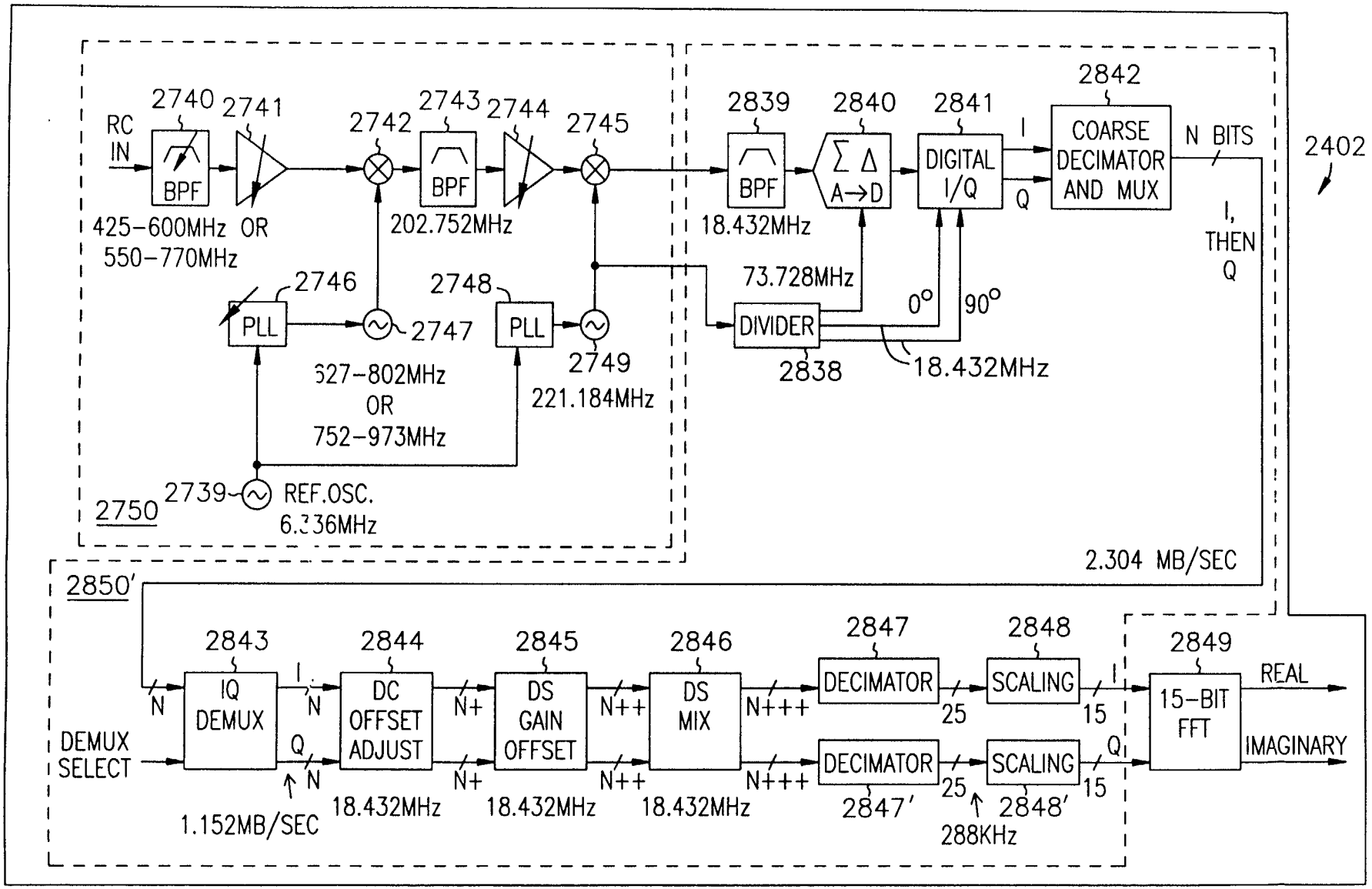

2402
RC IN
2740
2741
BPF
425-600MHz OR
550-770MHz
2742
2743
BPF
202.752MHz
2744
2745
2746
PLL
2747
527-802MHz
OR
752-973MHz
2748
PLL
2749
221.184MHz
2739
REF.OSC.
6.336MHz
2750
2839
BPF
18.432MHz
2840
Σ Δ
A→D
2841
DIGITAL
I/Q
I
Q
2842
COARSE
DECIMATOR
AND MUX
N BITS
I,
THEN
Q
73.728MHz
DIVIDER
2838
0°
90°
18.432MHz
2.304 MB/SEC
2850'
2843
IQ
DEMUX
DEMUX
SELECT
N
I
Q
N
1.152MB/SEC
2844
DC
OFFSET
ADJUST
18.432MHz
N+
2845
DS
GAIN
OFFSET
18.432MHz
N++
2846
DS
MIX
18.432MHz
N+++
2847
DECIMATOR
25
2847'
2848
SCALING
15
2848'
288KHz
2849
15-BIT
FFT
REAL
IMAGINARY

FIG. 94

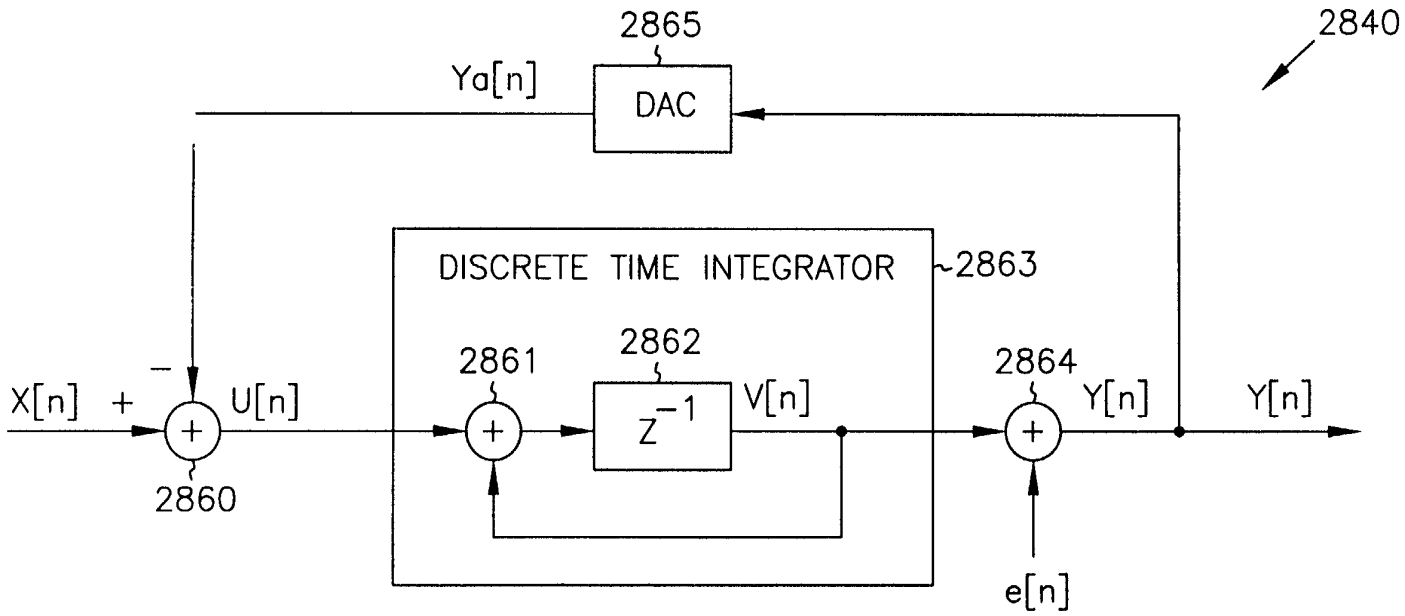

2865
2840
Ya[n]
DAC
DISCRETE TIME INTEGRATOR
2863
2861
2862
2864
X[n]
+
−
U[n]
V[n]
Y[n]
Y[n]
2860
e[n]

FIG. 95

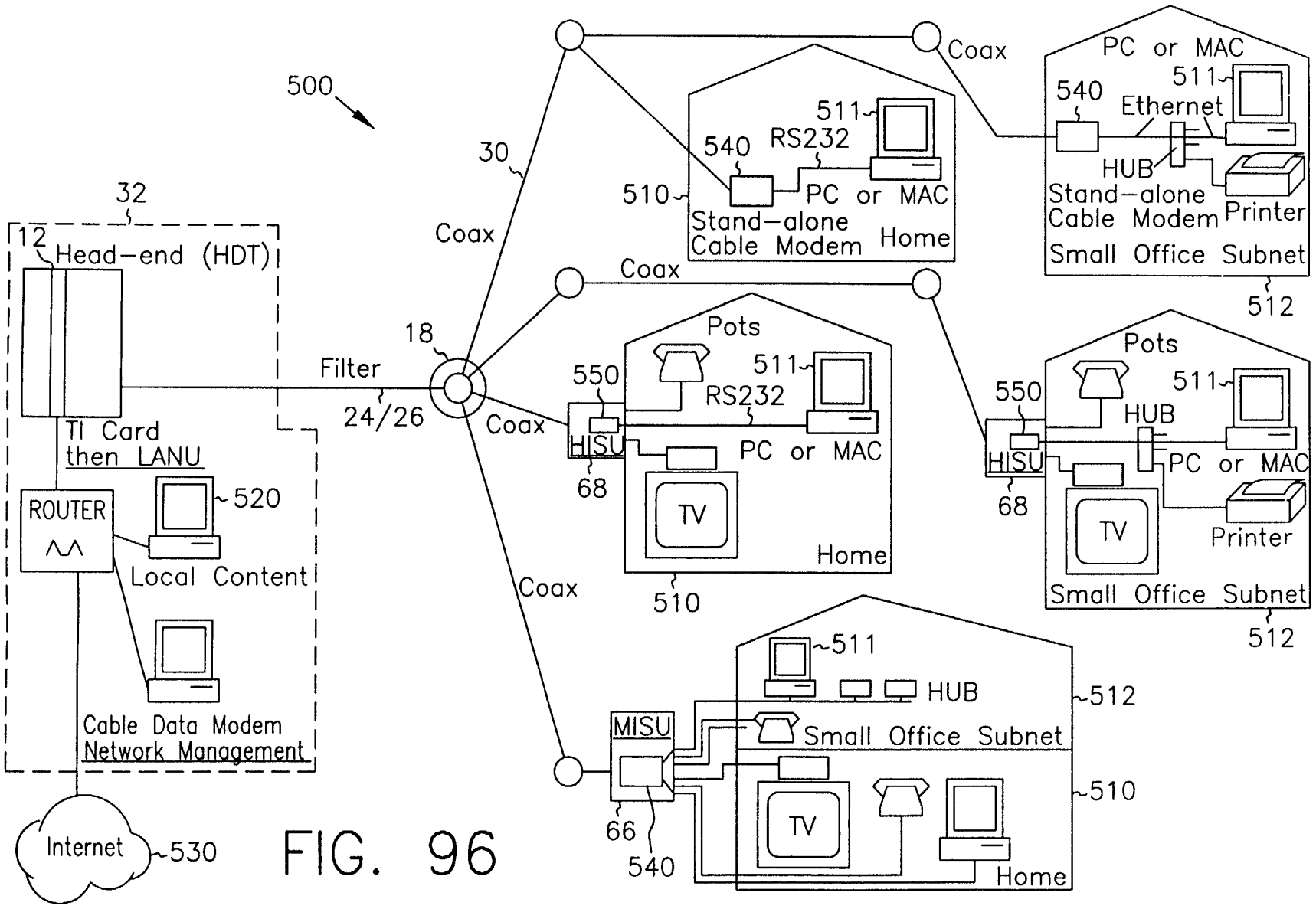

500
32
12
Head-end (HDT)
TI Card
then LANU
ROUTER
520
Local Content
Cable Data Modem
Network Management
Internet
530
Filter
24/26
18
30
Coax
Coax
Coax
Coax
Coax
Stand-alone
Cable Modem
510
540
RS232
511
PC or MAC
Home
PC or MAC
511
540
Ethernet
HUB
Stand-alone
Cable Modem
Printer
Small Office Subnet
512
Pots
550
511
RS232
HISU
68
PC or MAC
TV
Home
510
Pots
550
511
HUB
HISU
68
PC or MAC
TV
Printer
Small Office Subnet
512
MISU
66
540
511
HUB
512
Small Office Subnet
510
TV
Home

FIG. 96

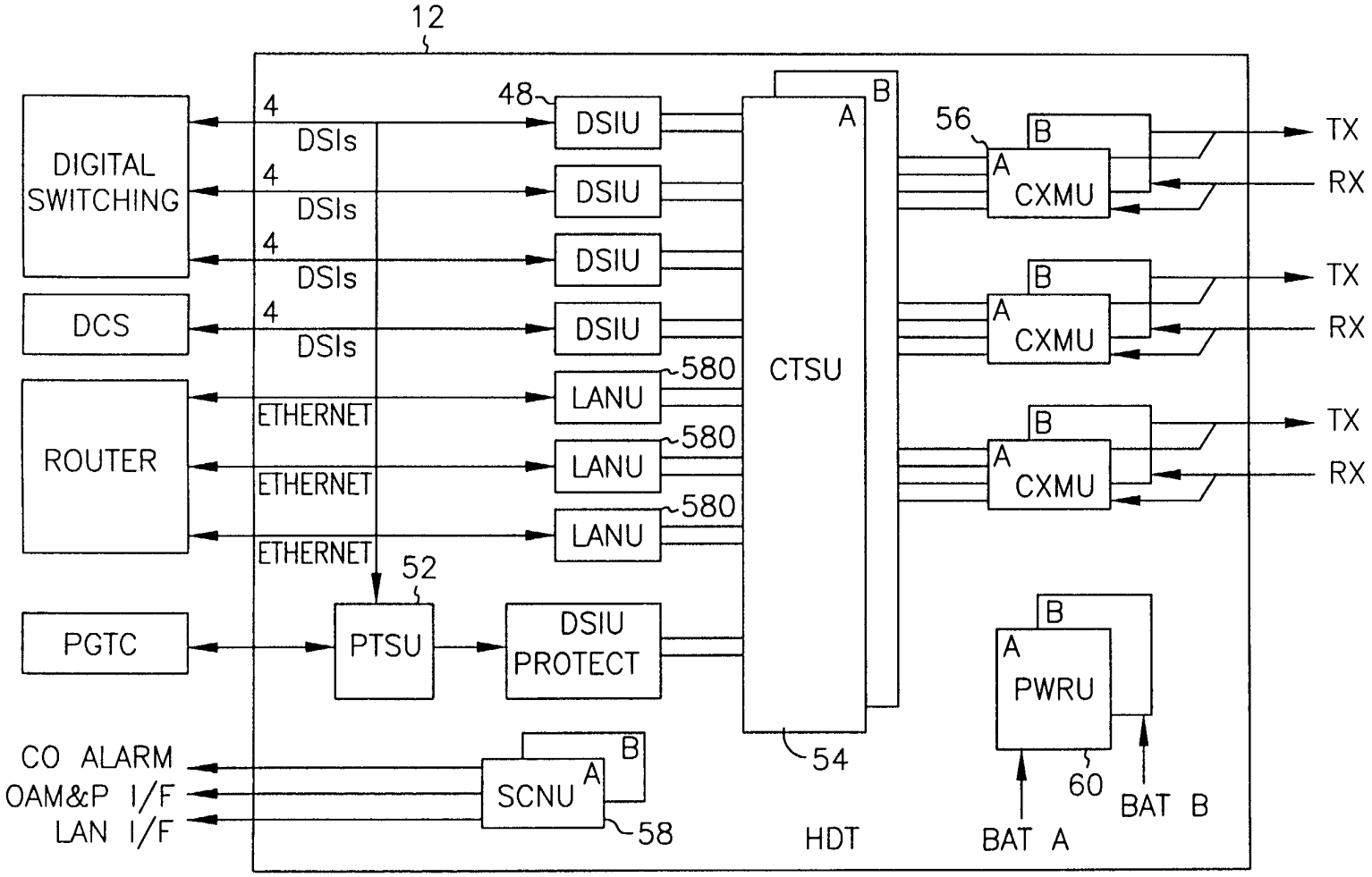

12
DIGITAL SWITCHING
DCS
ROUTER
PGTC
CO ALARM
OAM&P I/F
LAN I/F
4 DSIs
4 DSIs
4 DSIs
4 DSIs
ETHERNET
ETHERNET
ETHERNET
48
DSIU
DSIU
DSIU
DSIU
LANU
LANU
LANU
580
580
580
52
PTSU
DSIU PROTECT
SCNU
A
B
58
CTSU
54
HDT
56
CXMU
CXMU
CXMU
TX
RX
TX
RX
TX
RX
PWRU
60
BAT A
BAT B

FIG. 97

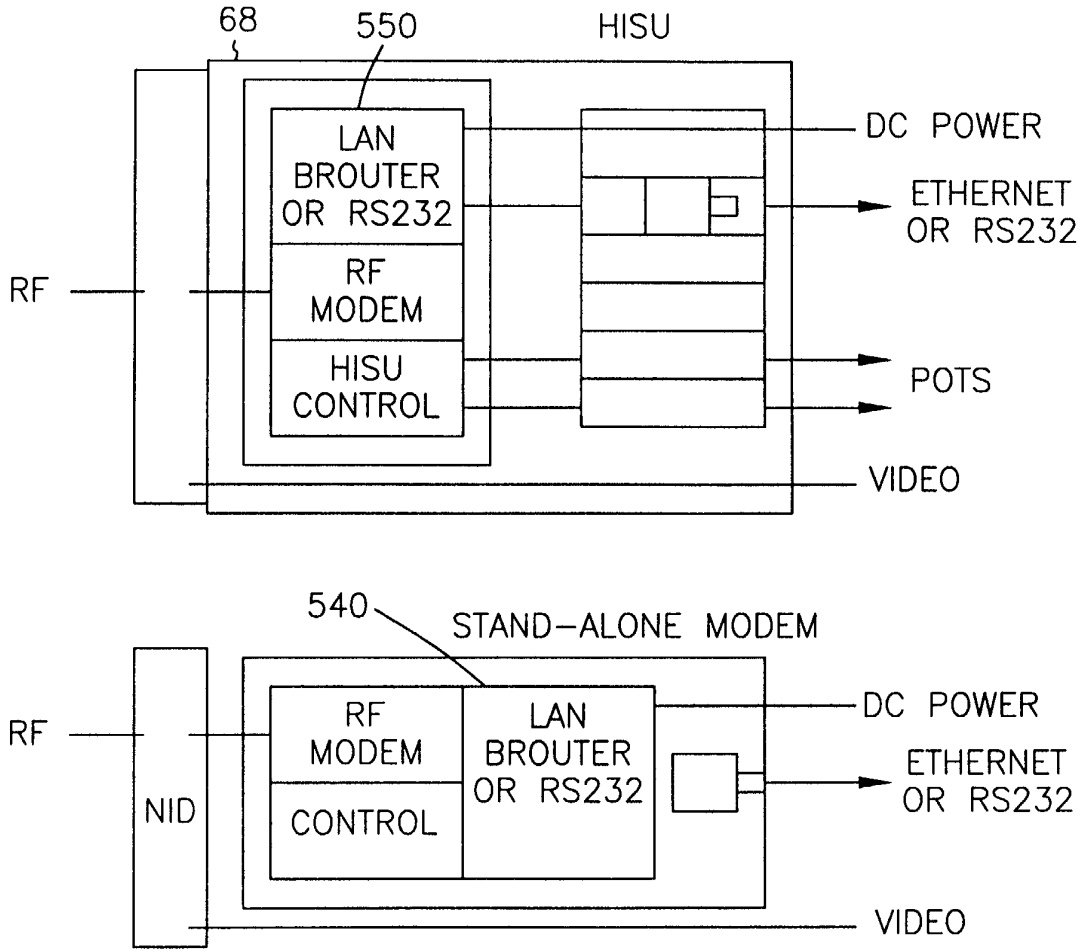

68
550
HISU
LAN
BROUTER
OR RS232
RF
MODEM
HISU
CONTROL
RF
DC POWER
ETHERNET
OR RS232
POTS
VIDEO
540
STAND-ALONE MODEM
RF
NID
RF
MODEM
CONTROL
LAN
BROUTER
OR RS232
DC POWER
ETHERNET
OR RS232
VIDEO

FIG. 98

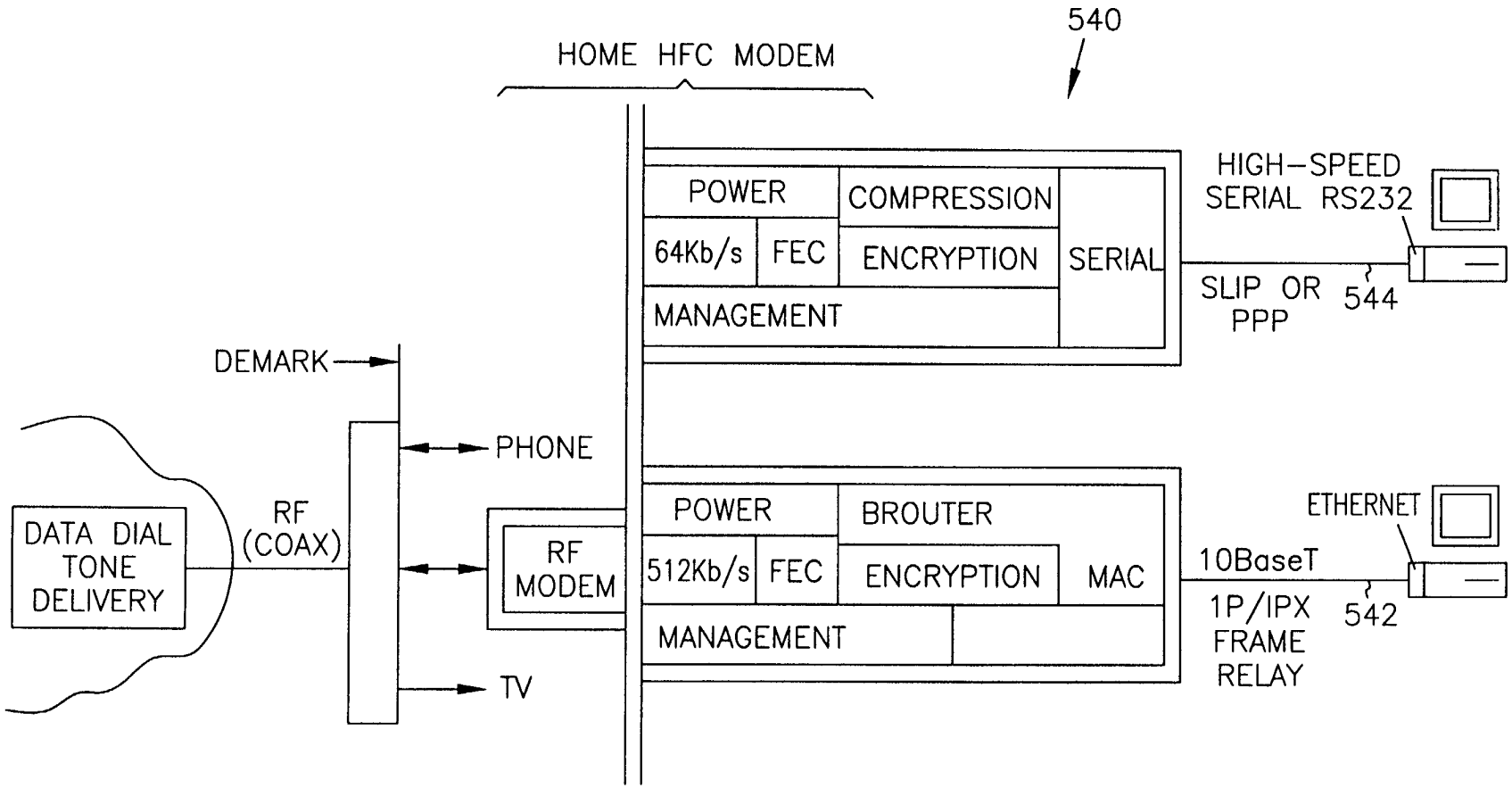

540
HOME HFC MODEM
POWER
COMPRESSION
64Kb/s
FEC
ENCRYPTION
SERIAL
MANAGEMENT
HIGH-SPEED SERIAL RS232
SLIP OR PPP
544
DEMARK
PHONE
DATA DIAL TONE DELIVERY
RF (COAX)
RF MODEM
POWER
BROUTER
512Kb/s
FEC
ENCRYPTION
MAC
MANAGEMENT
ETHERNET
10BaseT
1P/IPX FRAME RELAY
542
TV

FIG. 99

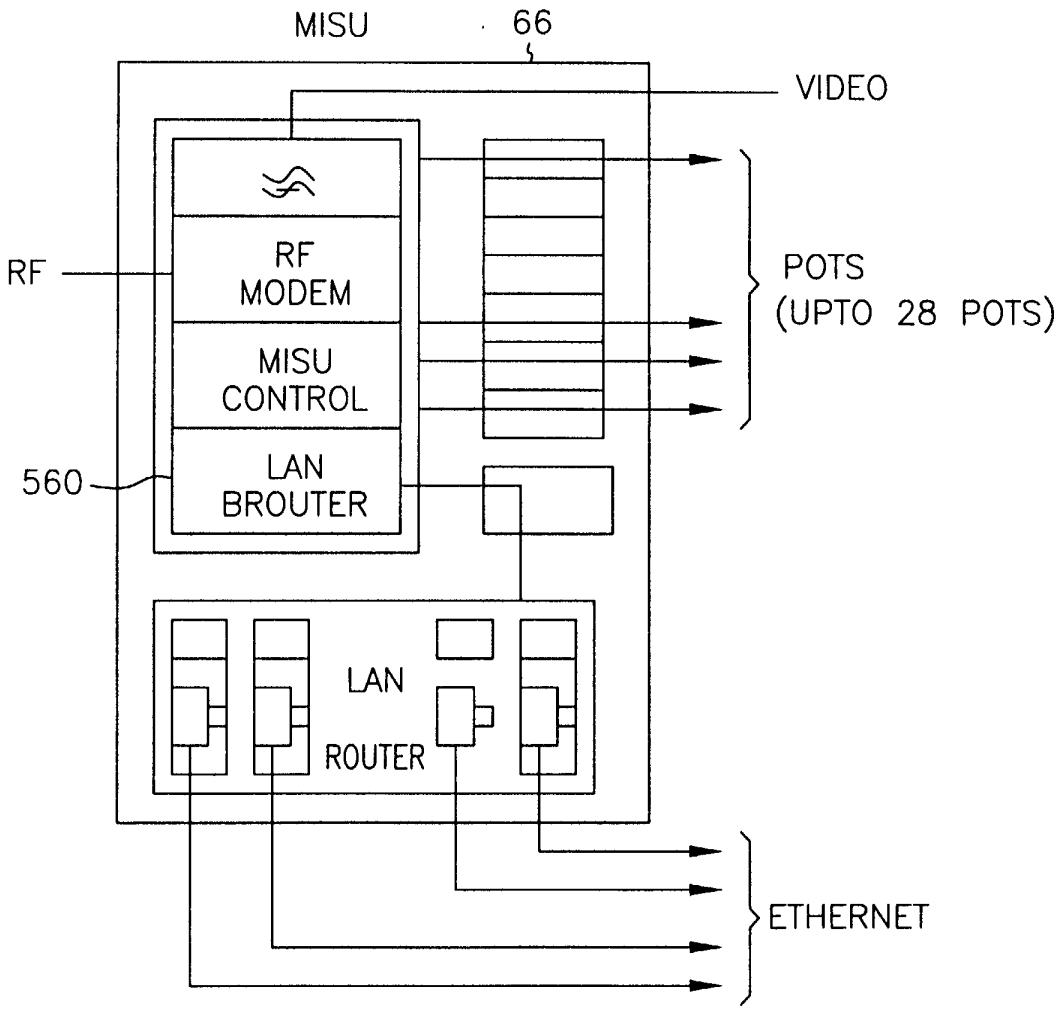

MISU
66
VIDEO
RF
RF MODEM
MISU CONTROL
LAN BROUTER
560
POTS
(UPTO 28 POTS)
LAN
ROUTER
ETHERNET

FIG. 100

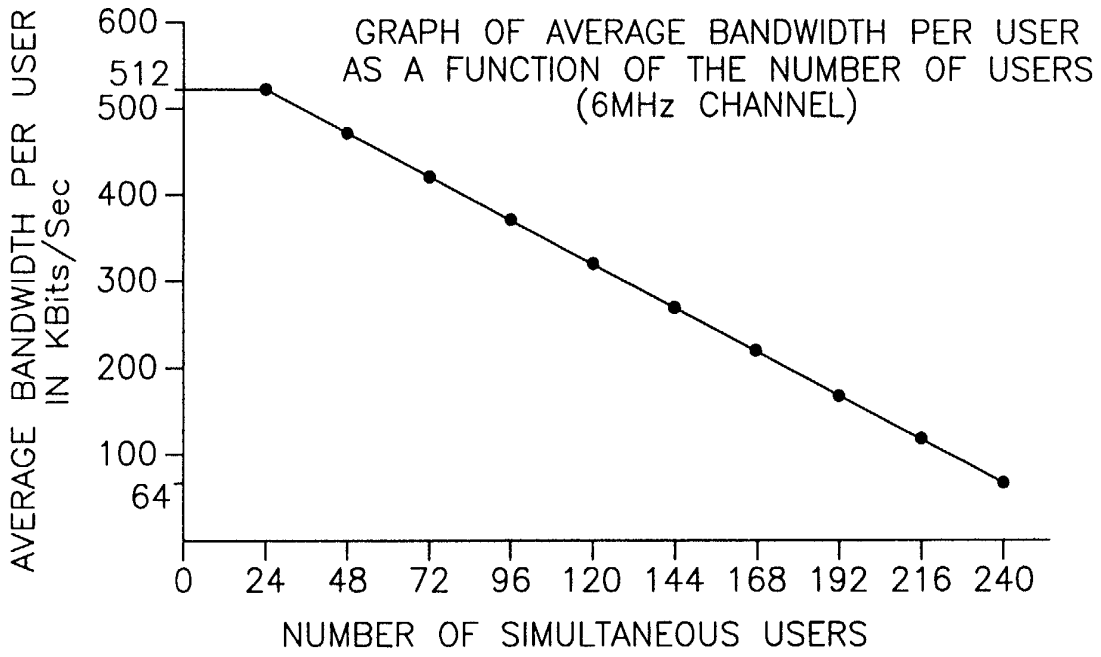

GRAPH OF AVERAGE BANDWIDTH PER USER
AS A FUNCTION OF THE NUMBER OF USERS
(6MHz CHANNEL)
AVERAGE BANDWIDTH PER USER
IN KBits/Sec
600
512
500
400
300
200
100
64
0
24
48
72
96
120
144
168
192
216
240
NUMBER OF SIMULTANEOUS USERS

FIG. 101

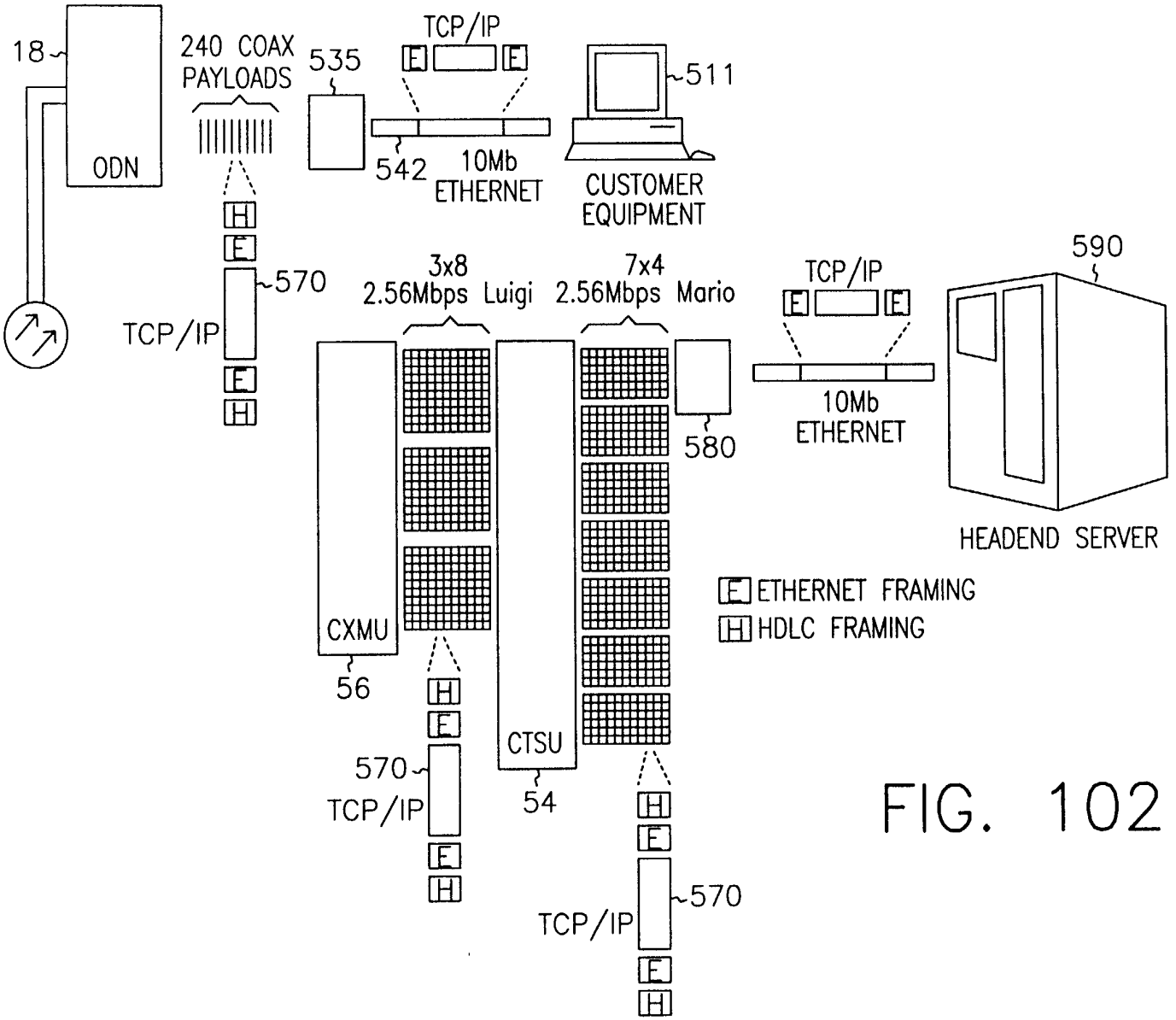

18
ODN
240 COAX PAYLOADS
535
TCP/IP
542
10Mb ETHERNET
511
CUSTOMER EQUIPMENT
590
HEADEND SERVER
570
TCP/IP
3x8 2.56Mbps Luigi
7x4 2.56Mbps Mario
580
CXMU
56
CTSU
54
ETHERNET FRAMING
HDLC FRAMING

FIG. 102

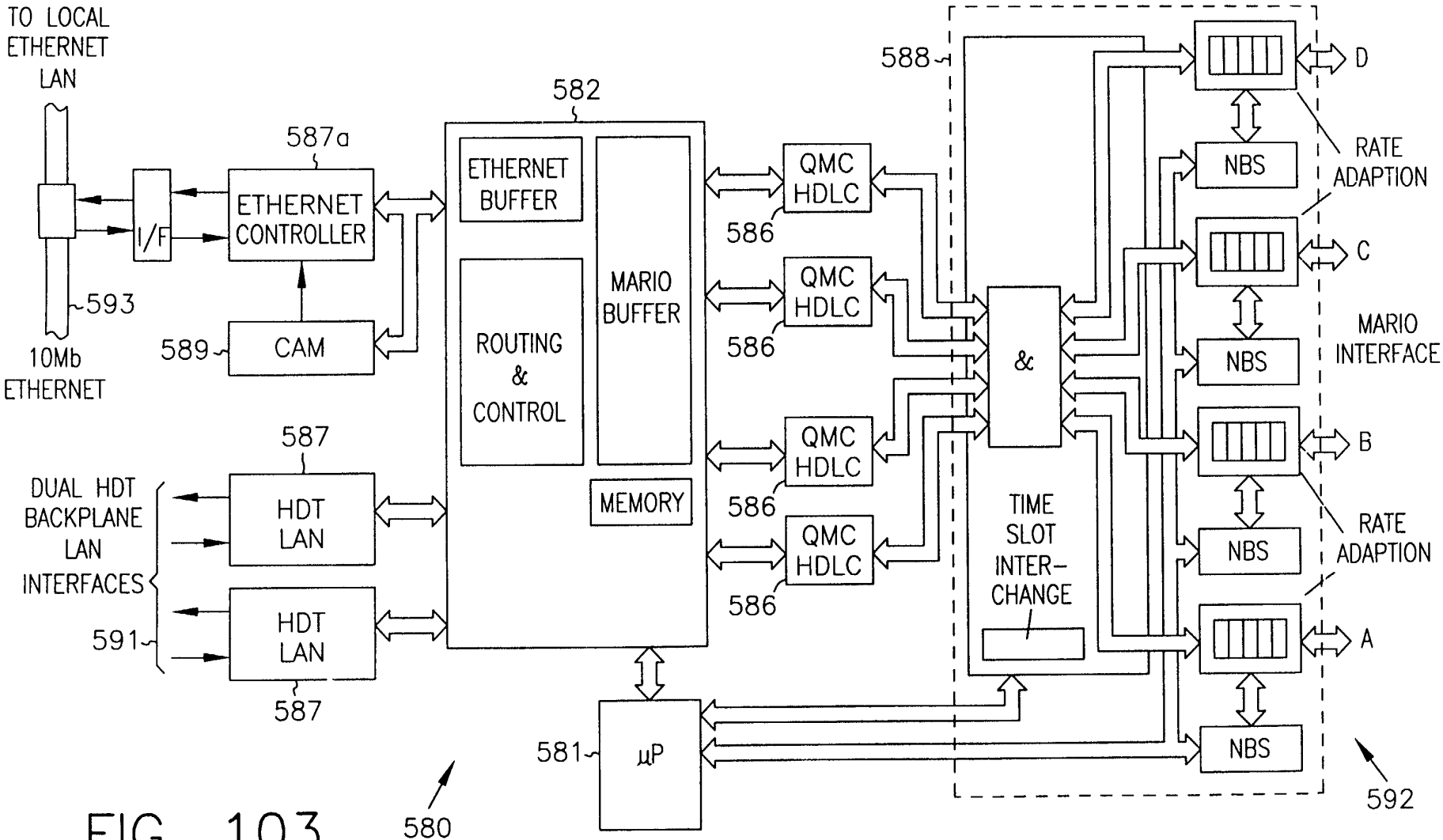

TO LOCAL ETHERNET LAN
10Mb ETHERNET
593
I/F
587a
ETHERNET CONTROLLER
589
CAM
582
ETHERNET BUFFER
ROUTING & CONTROL
MARIO BUFFER
MEMORY
586
QMC HDLC
586
QMC HDLC
586
QMC HDLC
586
QMC HDLC
588
&
TIME SLOT INTER-CHANGE
D
C
B
A
NBS
NBS
NBS
NBS
RATE ADAPTION
RATE ADAPTION
MARIO INTERFACE
587
DUAL HDT BACKPLANE LAN INTERFACES
591
HDT LAN
HDT LAN
587
581
µP
580
592

FIG. 103

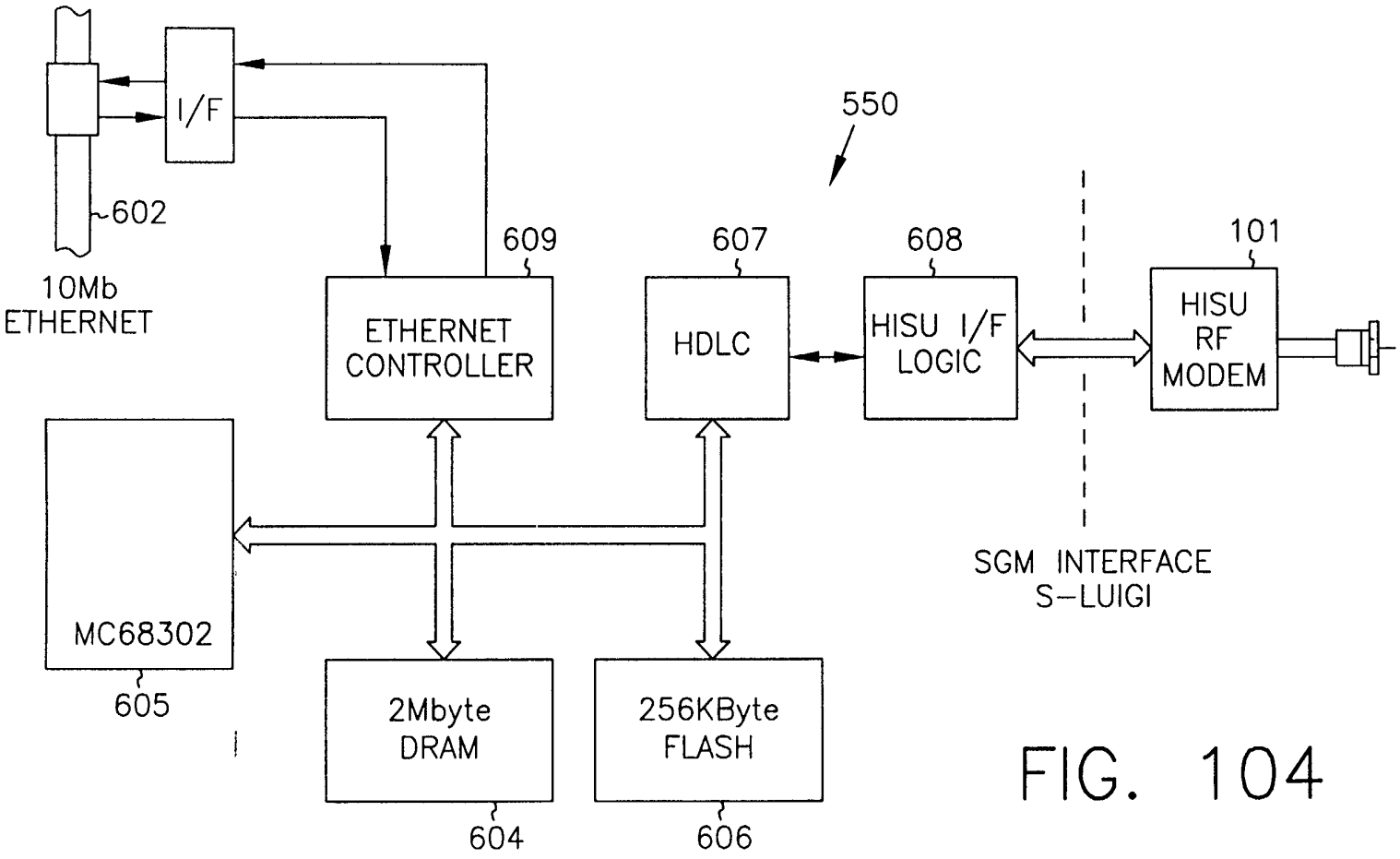

I/F
602
10Mb
ETHERNET
ETHERNET
CONTROLLER
609
550
607
HDLC
608
HISU I/F
LOGIC
101
HISU
RF
MODEM
SGM INTERFACE
S-LUIGI
MC68302
605
2Mbyte
DRAM
604
256KByte
FLASH
606

FIG. 104

TOSCO-HZ2E70660

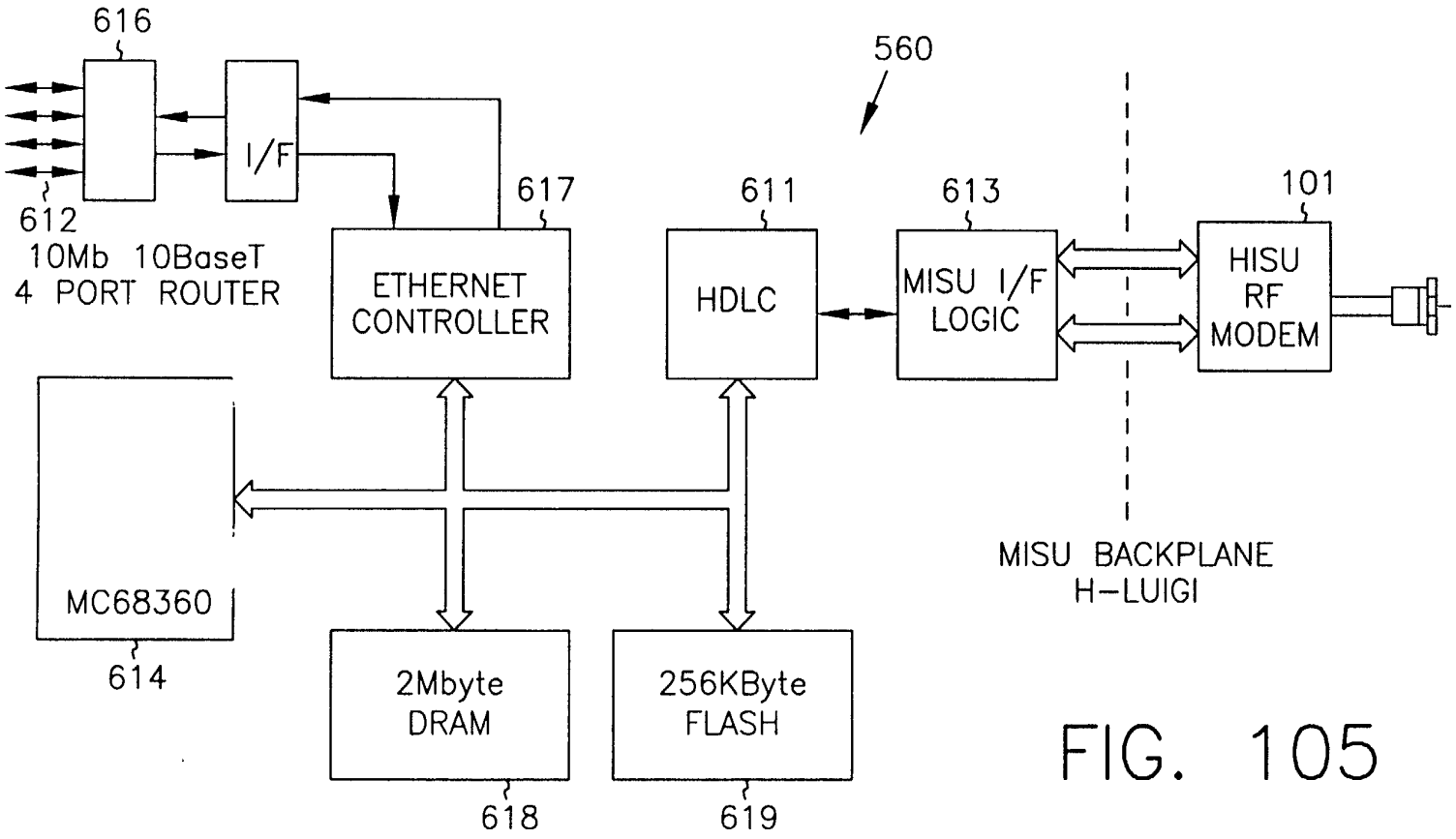


FIG. 105

T06020 "WZET0660

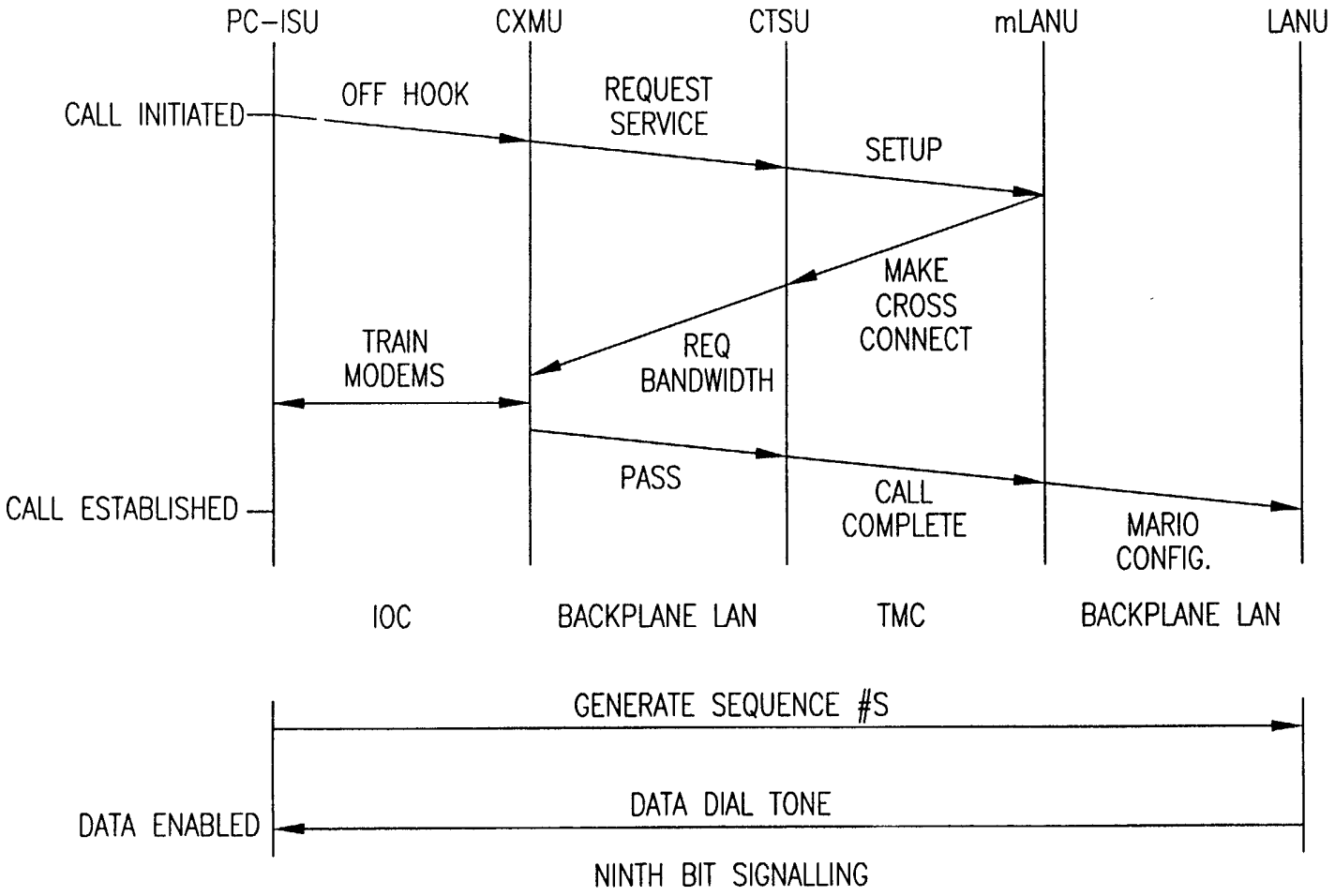


FIG. 106

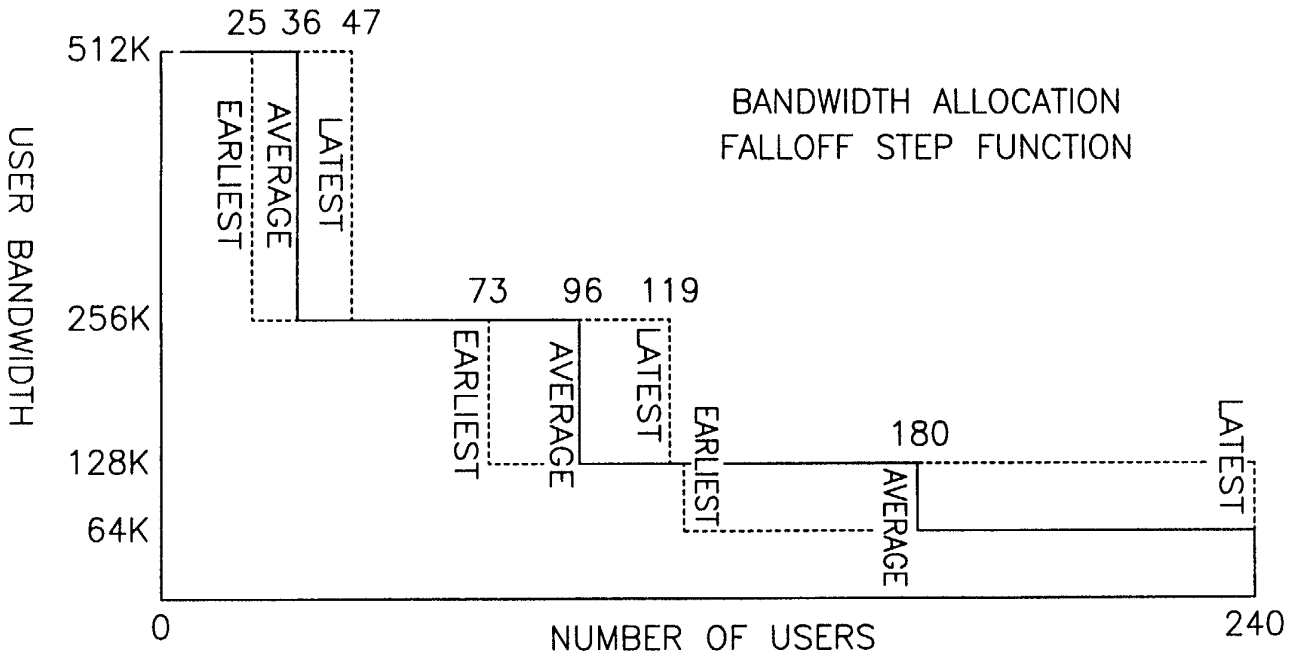
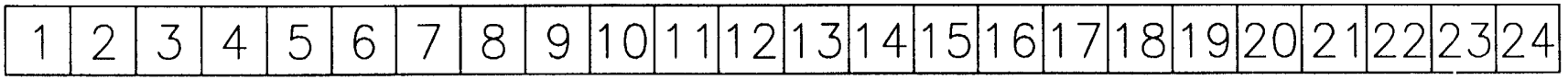
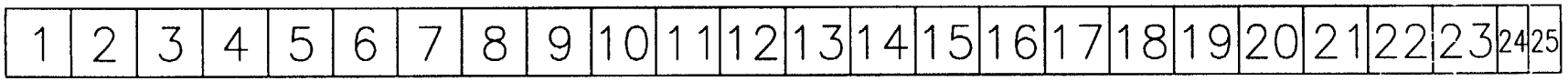

BANDWIDTH ALLOCATION
FALLOFF STEP FUNCTION
USER BANDWIDTH
512K
256K
128K
64K
0
25 36 47
73 96 119
180
EARLIEST
AVERAGE
LATEST
NUMBER OF USERS
240

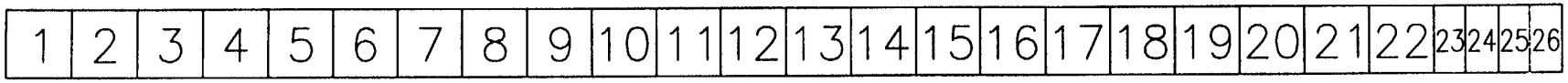
FIG. 107



THE RF SPECTRUM OF 24 USERS WITH 512Kbs



ADDING THE 25th USER



ADDING THE 26th USER, ETC

FIG. 108

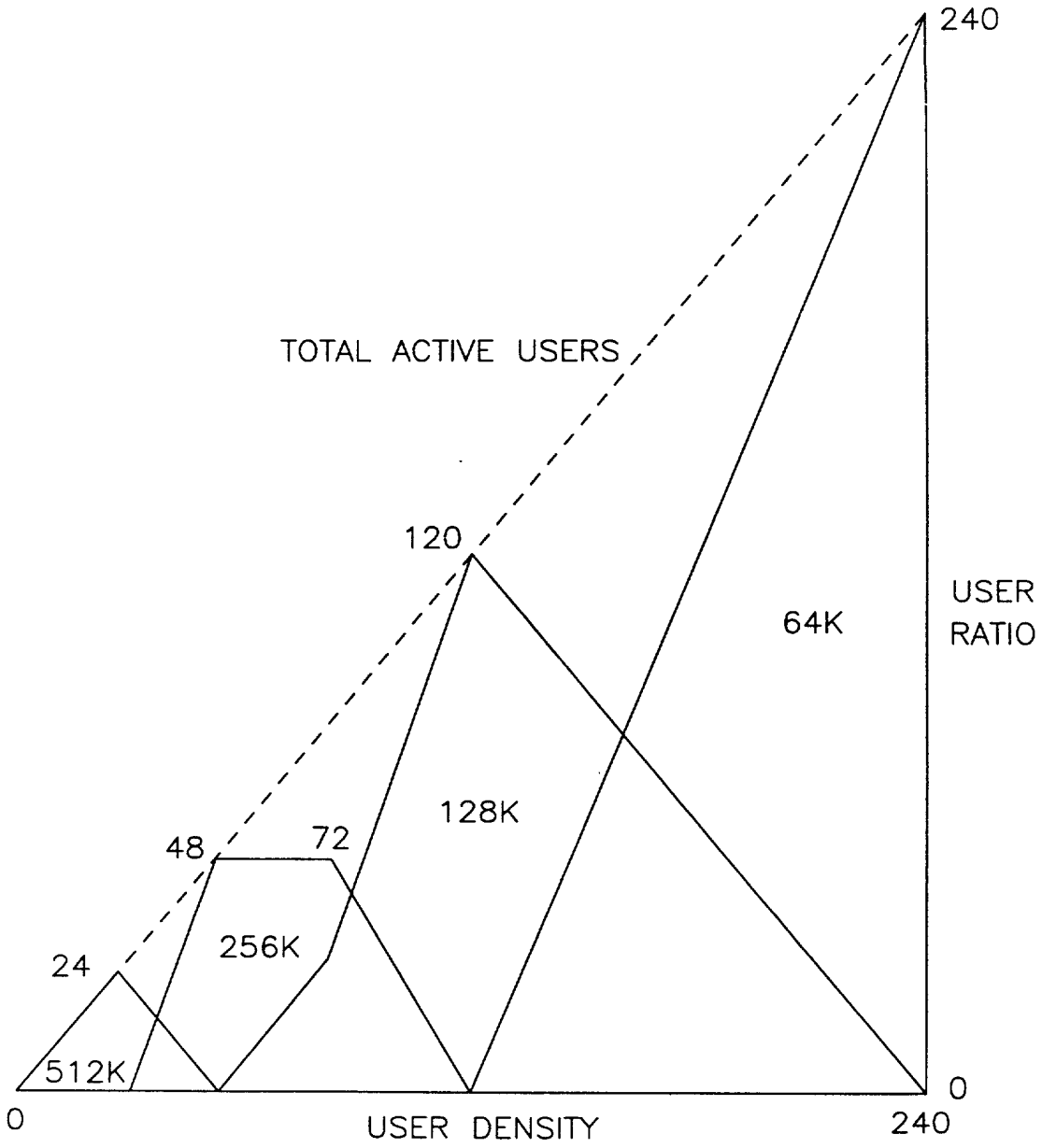

240
TOTAL ACTIVE USERS
120
64K
USER
RATIO
128K
48
72
256K
24
512K
0
0
USER DENSITY
240

FIG. 109

T06020"h2ET0660

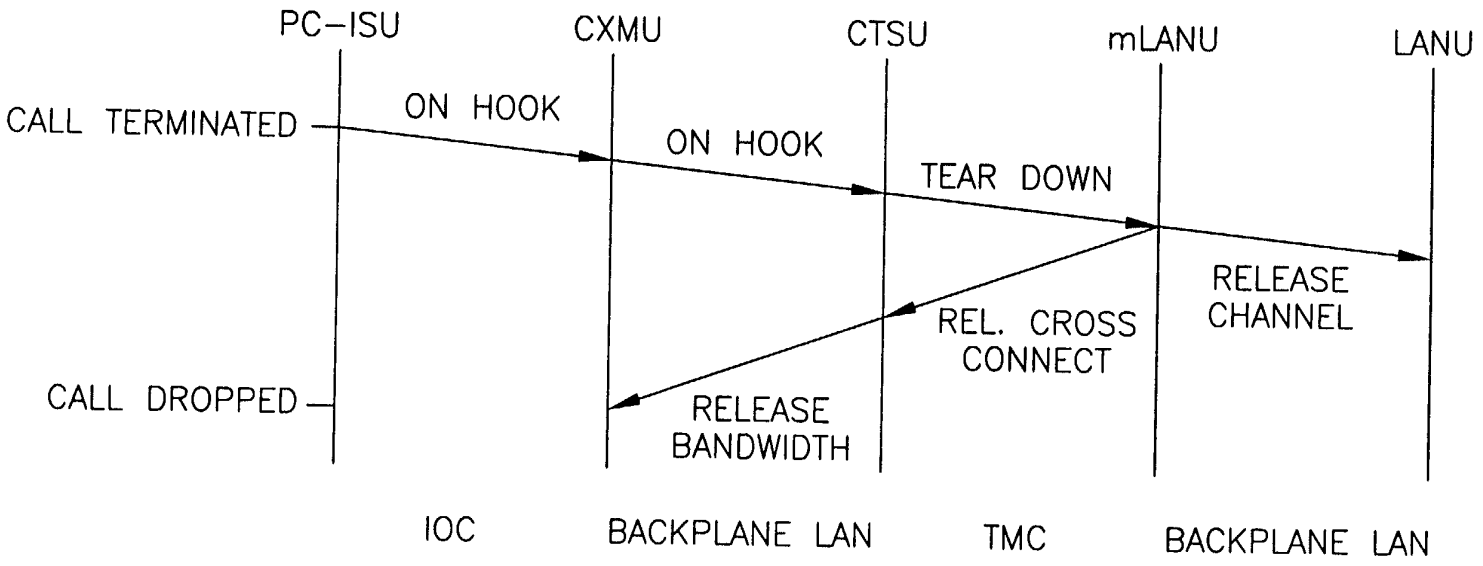


FIG. 110

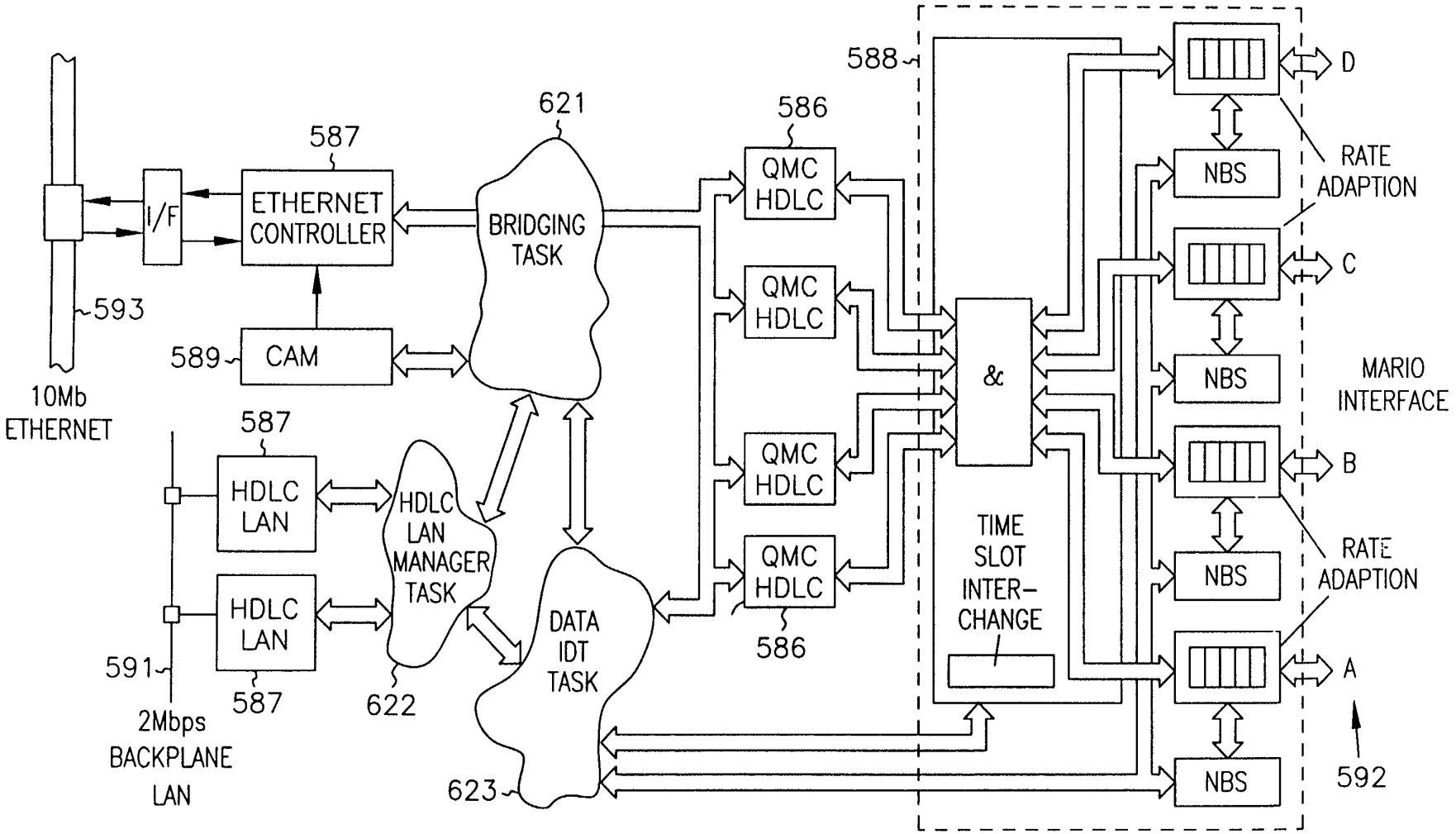

588
621
586
587
ETHERNET CONTROLLER
I/F
BRIDGING TASK
QMC HDLC
QMC HDLC
QMC HDLC
QMC HDLC
586
593
589
CAM
10Mb ETHERNET
&
D
C
B
A
NBS
NBS
NBS
NBS
RATE ADAPTION
RATE ADAPTION
MARIO INTERFACE
TIME SLOT INTER-CHANGE
587
HDLC LAN
HDLC LAN
HDLC LAN MANAGER TASK
DATA IDT TASK
591
2Mbps BACKPLANE LAN
587
622
623
592
620

FIG. 111

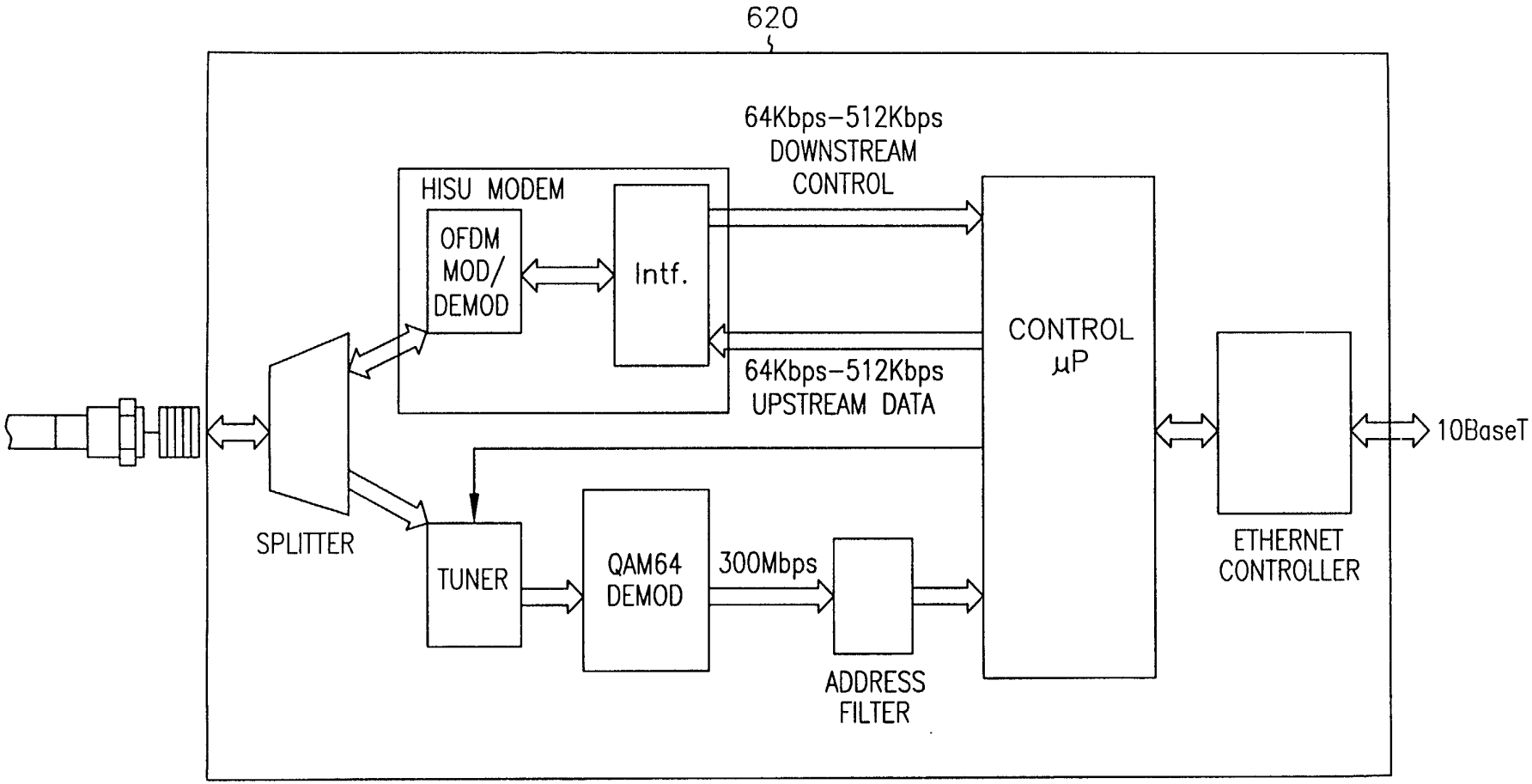

620
64Kbps–512Kbps
DOWNSTREAM
CONTROL
HISU MODEM
OFDM
MOD/
DEMOD
Intf.
CONTROL
μP
64Kbps–512Kbps
UPSTREAM DATA
10BaseT
SPLITTER
TUNER
QAM64
DEMOD
300Mbps
ADDRESS
FILTER
ETHERNET
CONTROLLER

FIG. 112

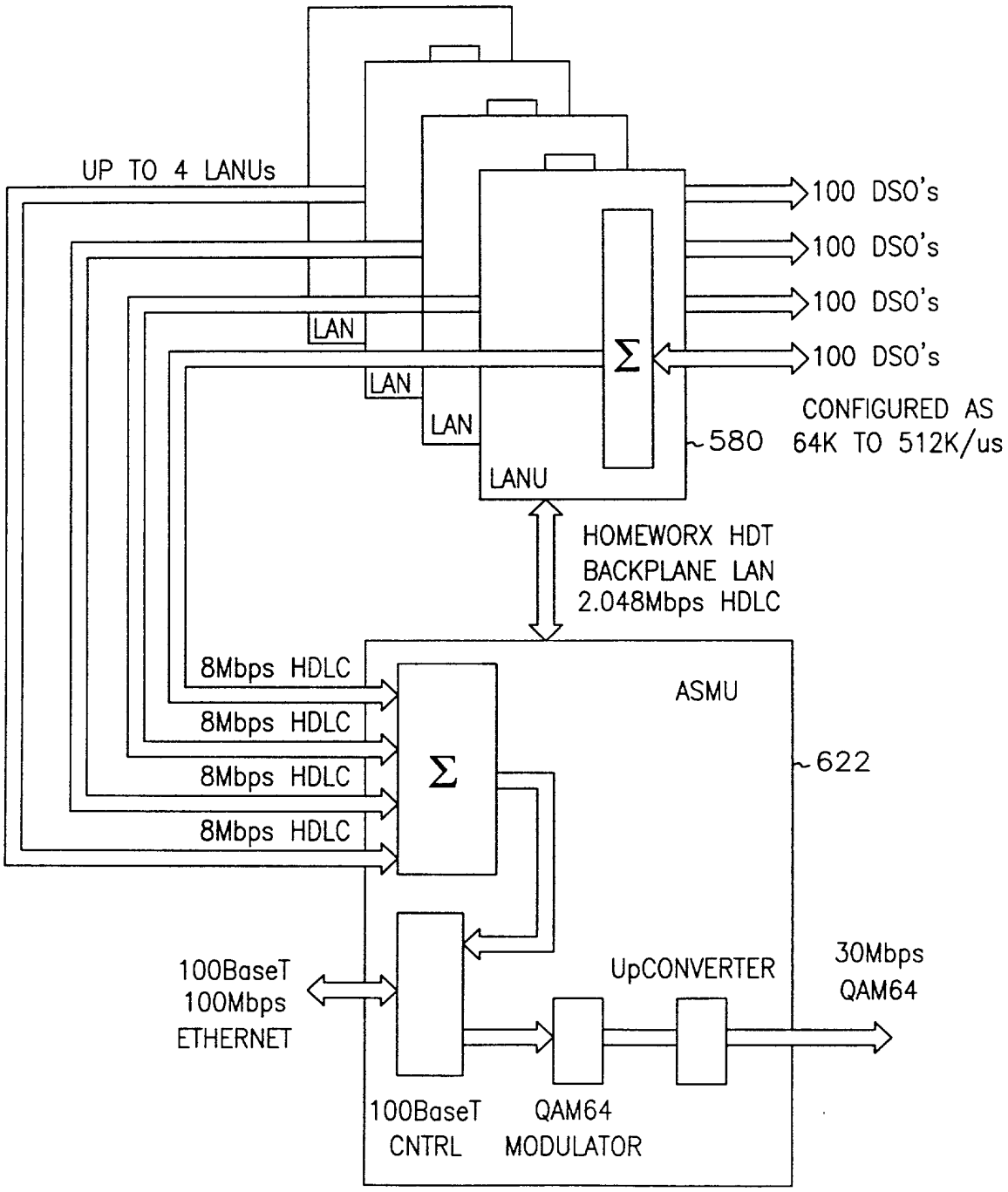

UP TO 4 LANUs
100 DSO's
100 DSO's
100 DSO's
100 DSO's
LAN
LAN
LAN
LANU
Σ
CONFIGURED AS
64K TO 512K/us
~580
HOMEWORX HDT
BACKPLANE LAN
2.048Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
Σ
ASMU
~622
100BaseT
100Mbps
ETHERNET
UpCONVERTER
30Mbps
QAM64
100BaseT
CNTRL
QAM64
MODULATOR

FIG. 113

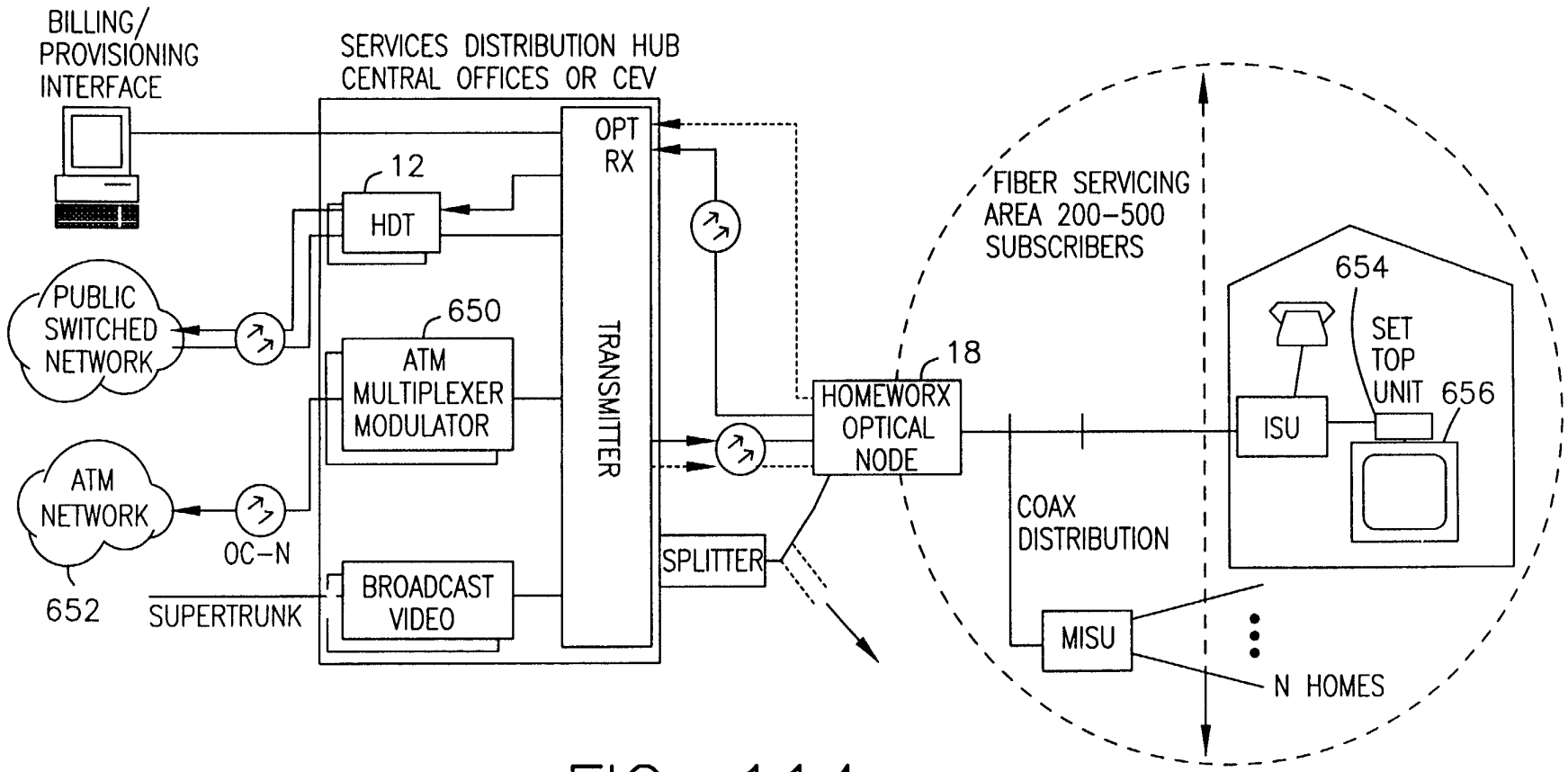

BILLING/
PROVISIONING
INTERFACE
SERVICES DISTRIBUTION HUB
CENTRAL OFFICES OR CEV
OPT
RX
12
HDT
PUBLIC
SWITCHED
NETWORK
650
ATM
MULTIPLEXER
MODULATOR
TRANSMITTER
ATM
NETWORK
OC-N
652
SUPERTRUNK
BROADCAST
VIDEO
SPLITTER
18
HOMEWORX
OPTICAL
NODE
FIBER SERVICING
AREA 200-500
SUBSCRIBERS
654
SET
TOP
UNIT
656
ISU
COAX
DISTRIBUTION
MISU
N HOMES

FIG. 114

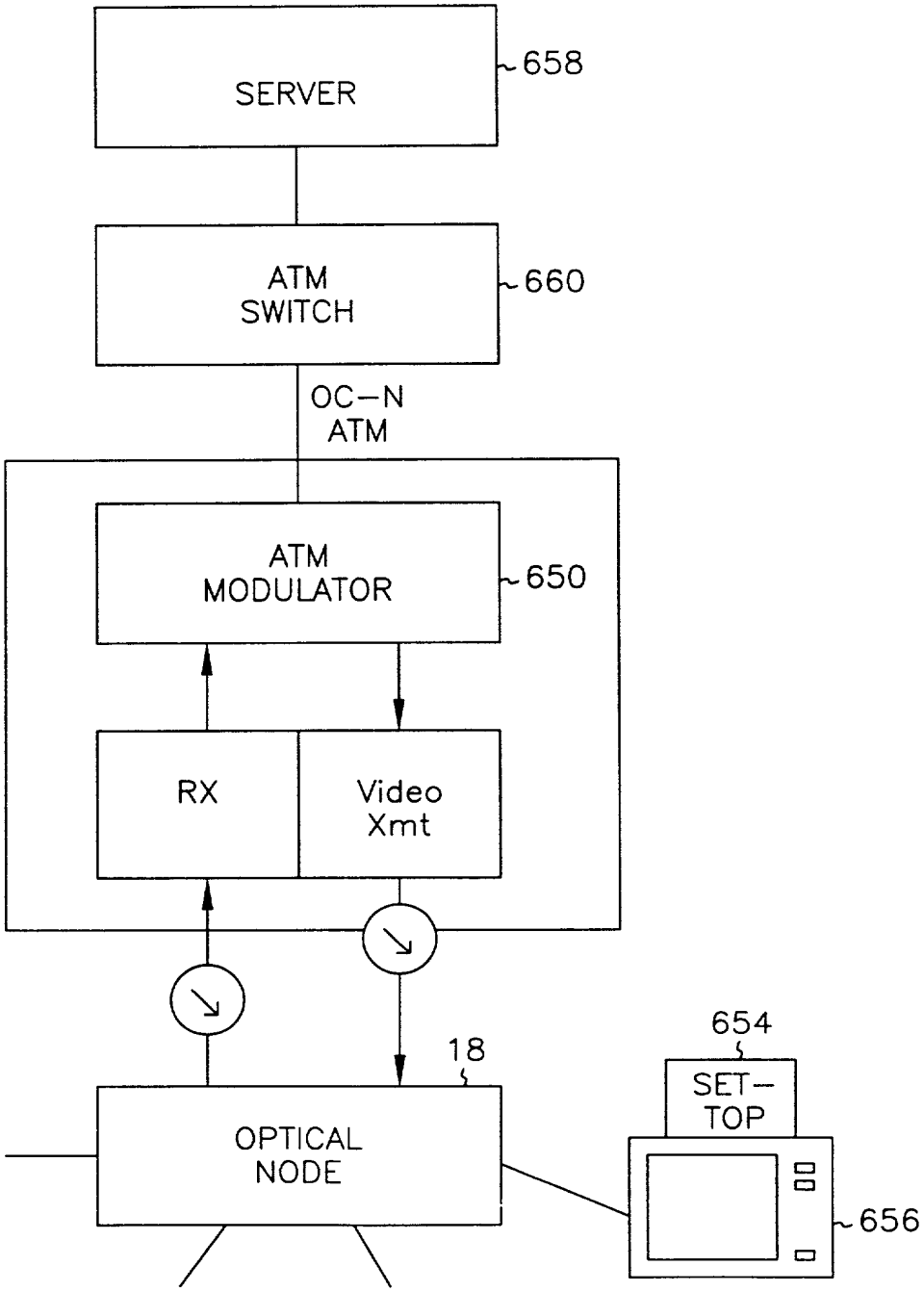

SERVER
658
ATM
SWITCH
660
OC–N
ATM
ATM
MODULATOR
650
RX
Video
Xmt
18
654
SET–
TOP
OPTICAL
NODE
656

FIG. 115

T0680 "h2ET0660

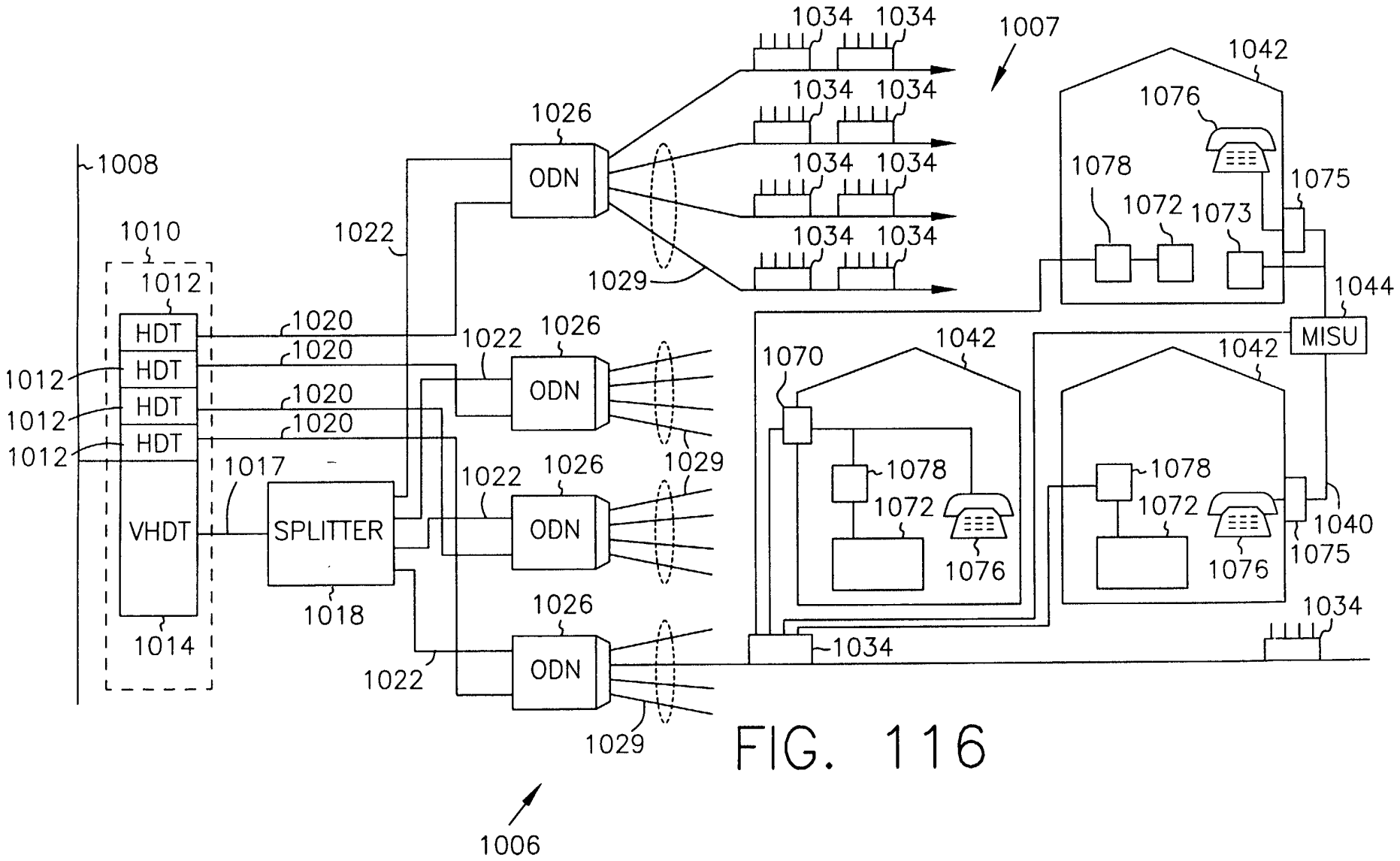


FIG. 116

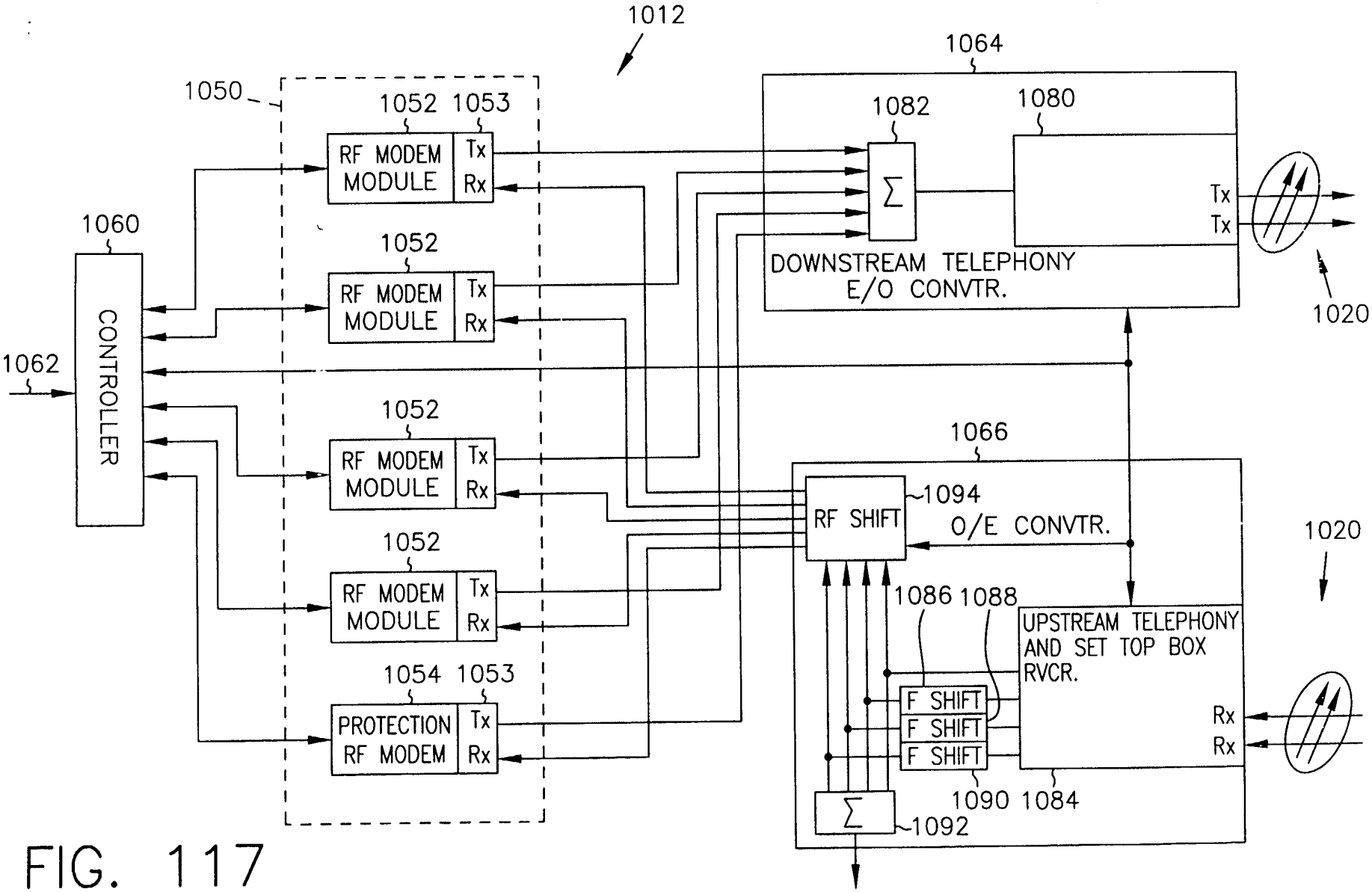

1012
1050
1052 1053
RF MODEM MODULE
Tx
Rx
1052
RF MODEM MODULE
Tx
Rx
1052
RF MODEM MODULE
Tx
Rx
1052
RF MODEM MODULE
Tx
Rx
1054 1053
PROTECTION RF MODEM
Tx
Rx
1060
CONTROLLER
1062
1064
1082
Σ
1080
Tx
Tx
DOWNSTREAM TELEPHONY E/O CONVTR.
1020
1066
RF SHIFT
1094
O/E CONVTR.
1020
1086 1088
UPSTREAM TELEPHONY AND SET TOP BOX RVCR.
F SHIFT
F SHIFT
F SHIFT
Rx
Rx
1090 1084
Σ
1092

FIG. 117

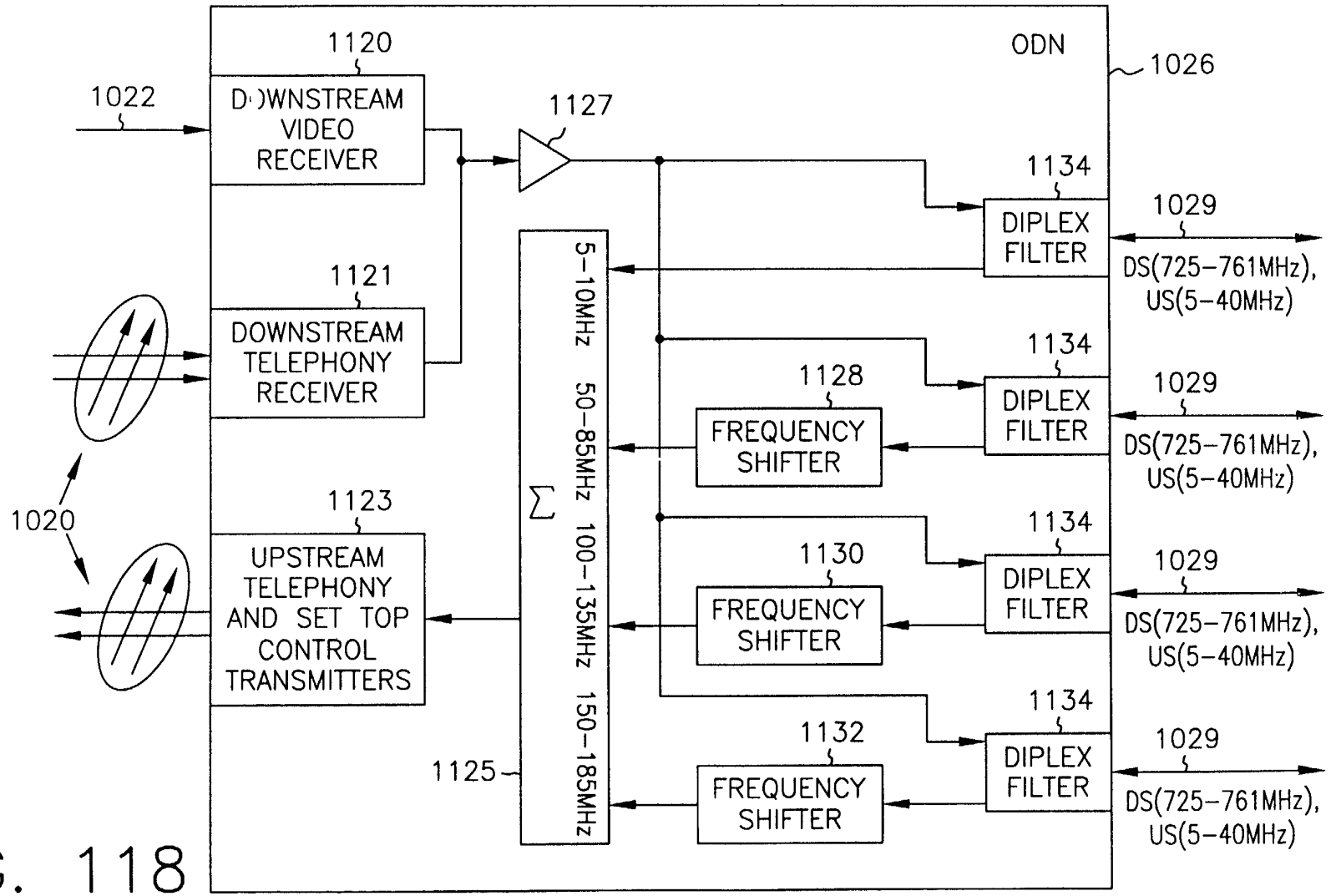

ODN
1026
1120
DOWNSTREAM VIDEO RECEIVER
1022
1127
1121
DOWNSTREAM TELEPHONY RECEIVER
1020
1123
UPSTREAM TELEPHONY AND SET TOP CONTROL TRANSMITTERS
1125
5–10MHz 50–85MHz 100–135MHz 150–185MHz
1134
DIPLEX FILTER
1029
DS(725–761MHz), US(5–40MHz)
1128
FREQUENCY SHIFTER
1130
1132

FIG. 118

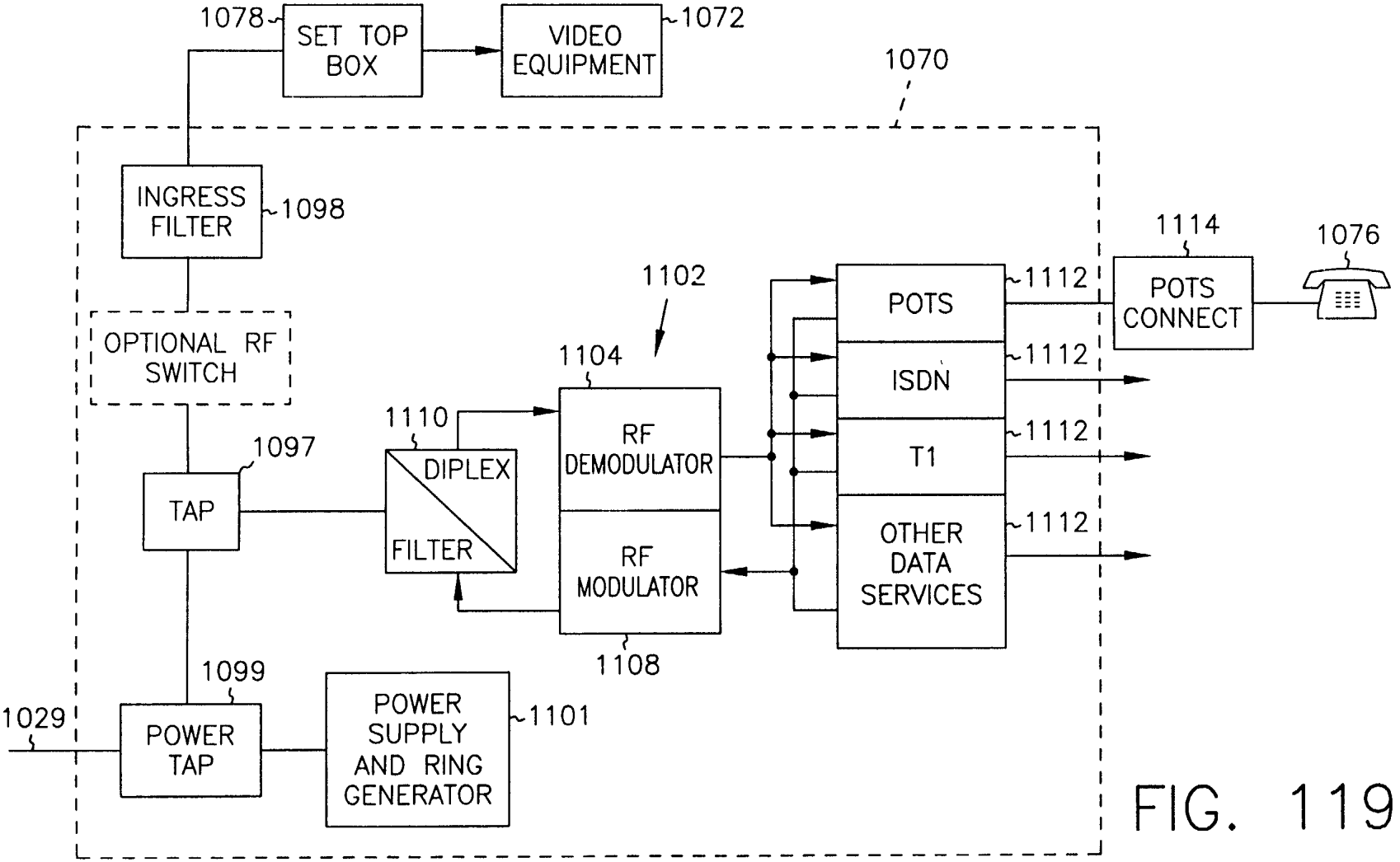

1078
SET TOP BOX
VIDEO EQUIPMENT
1072
1070
INGRESS FILTER
1098
OPTIONAL RF SWITCH
1097
TAP
1110
DIPLEX
FILTER
1102
1104
RF DEMODULATOR
RF MODULATOR
1108
POTS
ISDN
T1
OTHER DATA SERVICES
1112
1114
POTS CONNECT
1076
1029
1099
POWER TAP
POWER SUPPLY AND RING GENERATOR
1101

FIG. 119

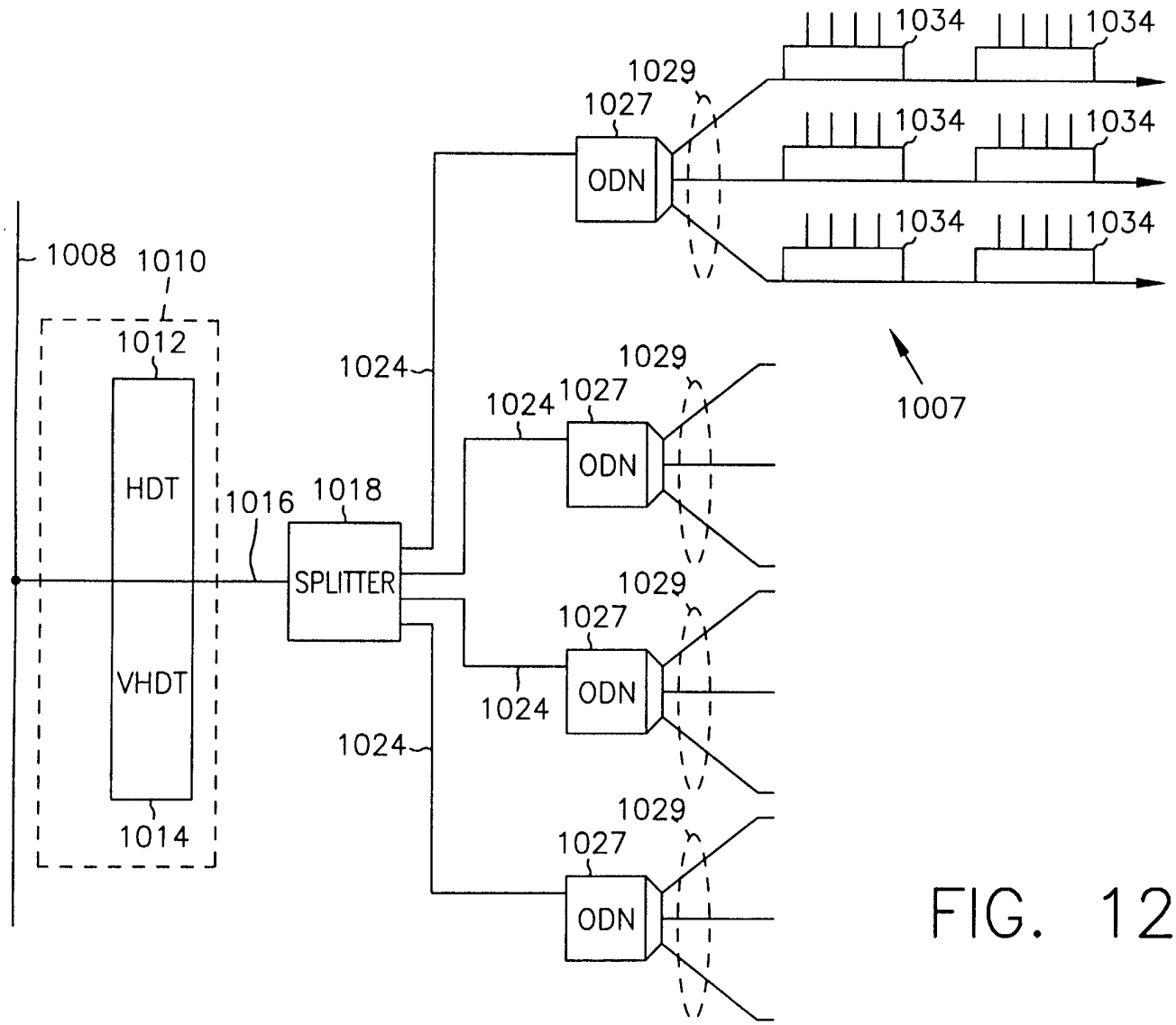

1034
1034
1029
1027
1034
1034
ODN
1034
1034
1008
1010
1012
1024
1029
1027
1024
ODN
1007
HDT
1016
1018
SPLITTER
1029
1027
VHDT
1024
ODN
1024
1029
1027
1014
ODN

FIG. 120

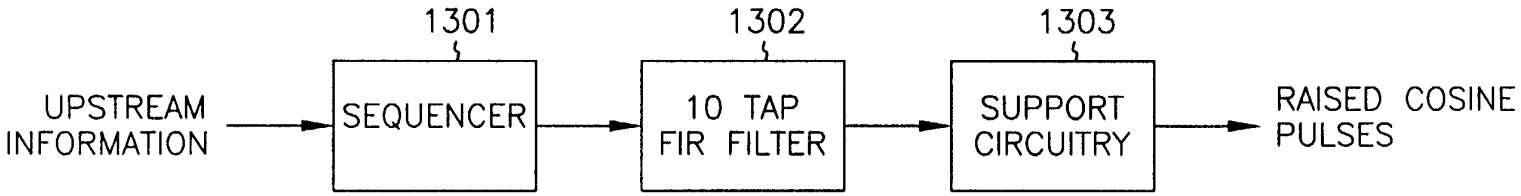

1301
1302
1303
UPSTREAM INFORMATION
SEQUENCER
10 TAP FIR FILTER
SUPPORT CIRCUITRY
RAISED COSINE PULSES

FIG. 121

09901370 "07090

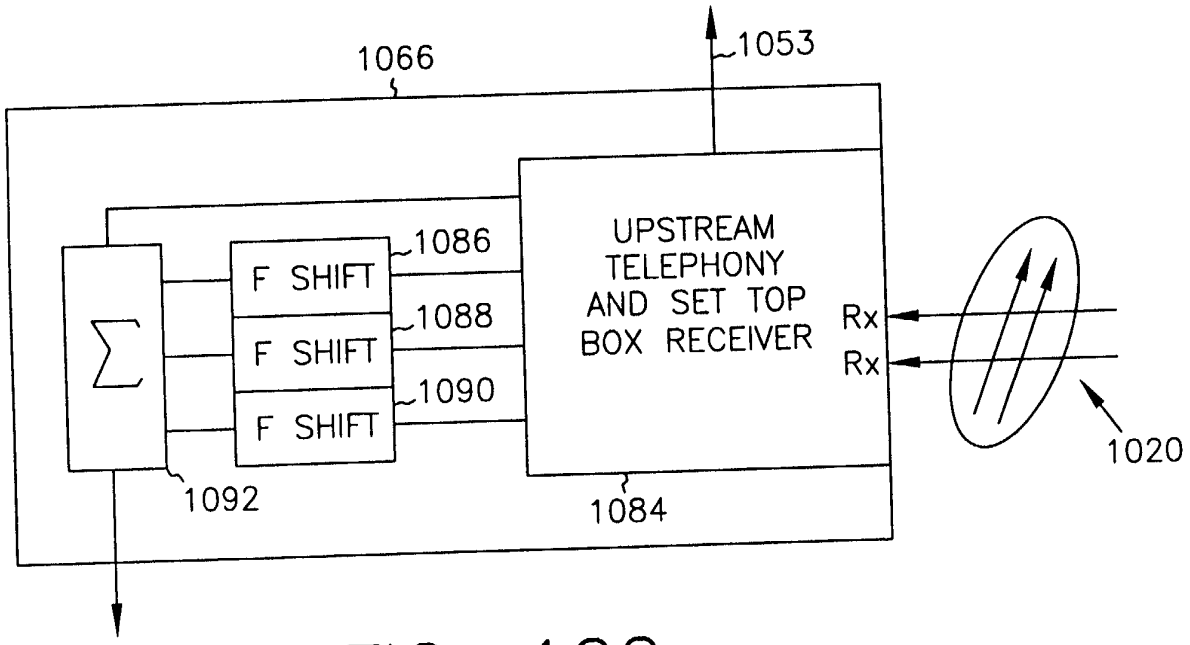


FIG. 122

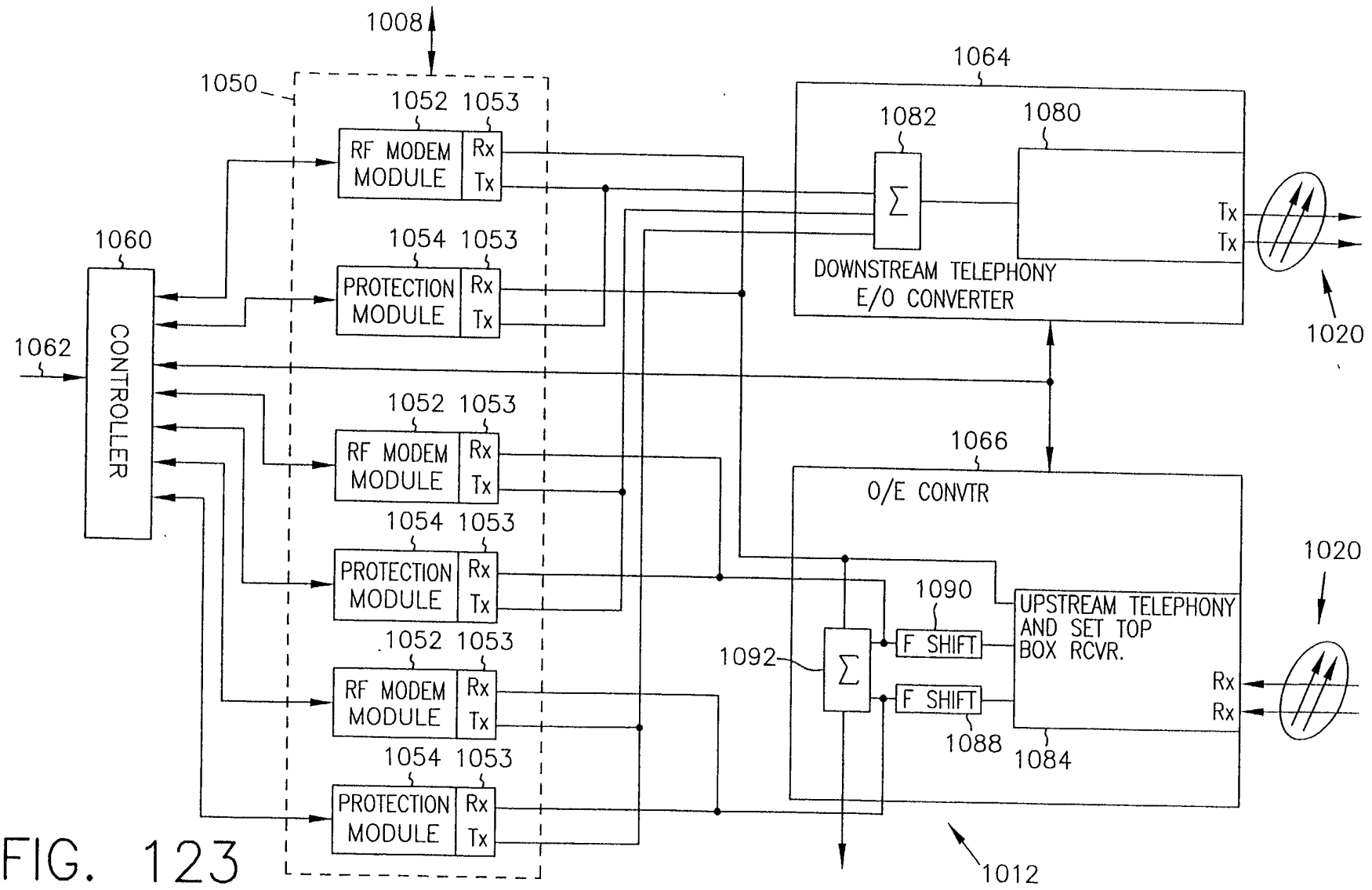

1008
1050
1052 1053
RF MODEM MODULE
Rx
Tx
1054 1053
PROTECTION MODULE
1060
CONTROLLER
1062
1064
1082
1080
Σ
DOWNSTREAM TELEPHONY E/O CONVERTER
Tx
Tx
1020
1066
O/E CONVTR
1090
F SHIFT
1092
UPSTREAM TELEPHONY AND SET TOP BOX RCVR.
Rx
Rx
1088
1084
1012

FIG. 123